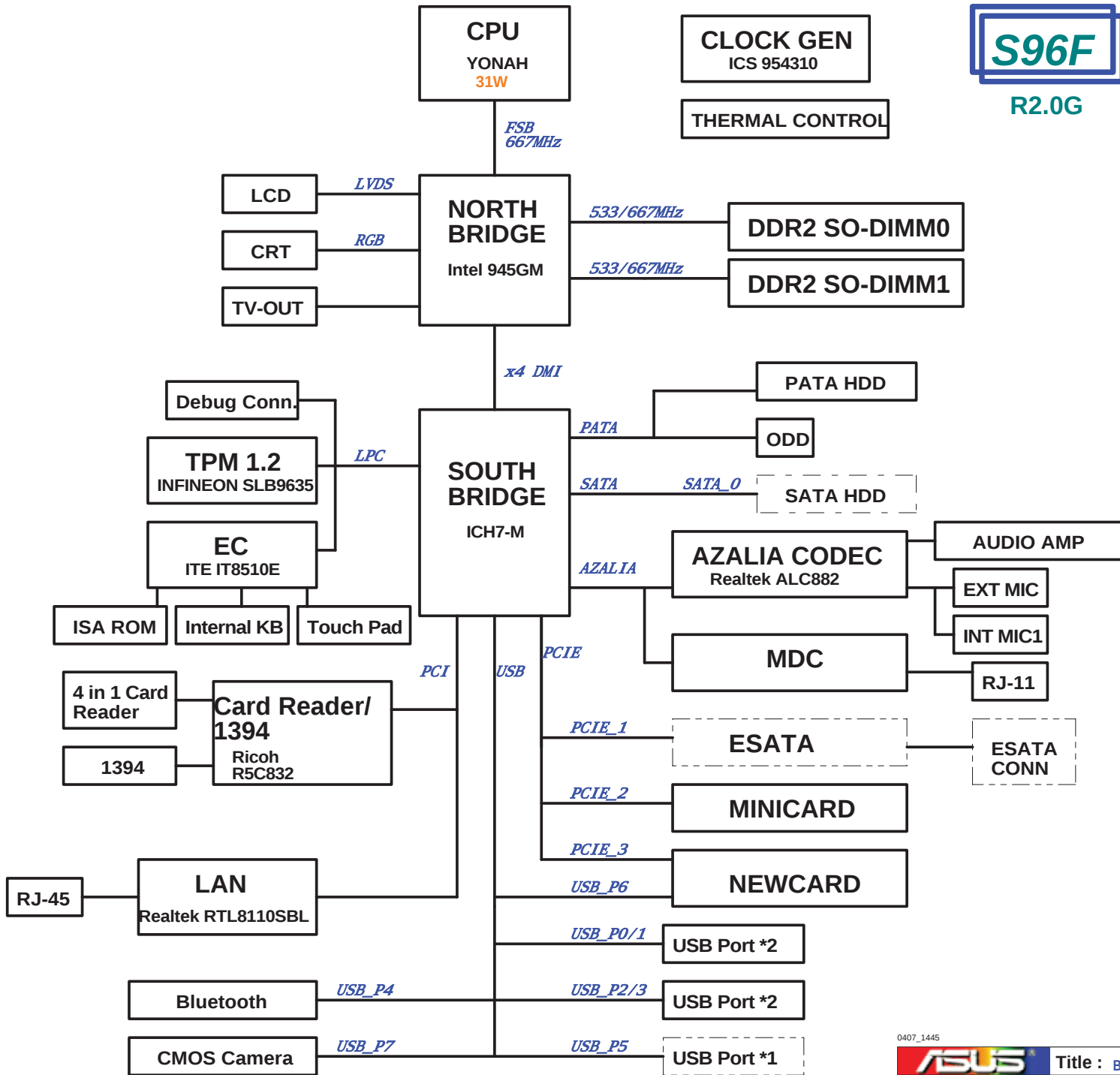


01\_Block Diagram  
02\_System Setting  
04\_CPU-YONAH(HOST)  
05\_CPU-YONAH(PWR)  
07\_NB-945GM(HOST)  
08\_NB-945GM(DMI & CFG)  
09\_NB-945GM(GRAPHIC)  
10\_NB-945GM(DDR2)  
11\_NB-945GM(PWR)  
12\_NB-945GM(PWR2)  
13\_NB-945GM(GND)  
15\_SB-ICH7M(1)  
16\_SB-ICH7M(2)  
17\_SB-ICH7M(3)  
18\_SB-ICH7M(PWR)  
20\_DDR2 SO-DIMM0  
21\_DDR2 SO-DIMM1  
22\_DDR2 TERMINATION  
32\_CRT  
33\_LVDS & INVERTER CONNECTOR  
35\_TV OUT CONN  
37\_THER SENSOR & FAN  
39\_CLOCK GEN-ICS954310  
41\_SWITCH  
42\_DISCHARGE  
44\_LAN-RTL8110SBL  
45\_MDC&RJ45&RJ11  
47\_MINI CARD  
49\_CARD1394-R5C832(1)  
50\_CARD1394-R5C832(2)  
51\_4 in 1 CARD READER  
52\_NEWCARD  
54\_PORT BAR  
56\_CODEC-ALC882  
57\_AUDIO AMP & JCAK  
59\_EC-IT8510E  
60\_Touch Pad & KB  
62\_USB CONN  
64\_ISA ROM  
66\_LED  
68\_DC & BAT IN  
70\_Debug CONN.  
72\_SATA-HDD & ODD  
74\_SREW HOLE  
76\_TPM  
78\_BT  
80\_POWER\_VCORE  
81\_POWER\_SYSTEM\_+3VO & +5VO  
82\_POWER\_I/O\_1.5VS & 1.15VS  
83\_POWER\_I/O\_DDR & VTT  
84\_POWER\_I/O\_+3VAO & +2.5VS  
87\_POWER\_CHARGER  
89\_POWER\_DETECT  
90\_POWER\_PROTECT  
91\_POWER\_LOAD SWITCH  
92\_POWER\_FLOWCHART  
93\_POWER\_SIGNAL  
94\_History (1)  
95\_History (2)



EC GPIO SETTING

| Pin | Pin Name          | Signal Name   | Type    | Default | EC Default |
|-----|-------------------|---------------|---------|---------|------------|
| 32  | PWM0/GPA0         | /             |         |         | GPI        |
| 33  | PWM1/GPA1         | FAN_PWM       | O       | H       | GPI        |
| 36  | PWM2/GPA2         | CLK_PWRSERVE# | O       | H       | GPI        |
| 37  | PWM3/GPA3         | /             | I       |         | GPI        |
| 38  | PWM4/GPA4         | CHG_LED_UP#   | O       | H       | GPI        |
| 39  | PWM5/GPA5         | PWR_LED_UP#   | O       | H       | GPI        |
| 40  | PWM6/GPA6         | /             | O       |         | GPI        |
| 43  | PWM7/GPA7         | LCD_BACKOFF#  | O       | H       | GPI        |
| 153 | RXD/GPB0          | NUM_LED       | O       | L       | GPI        |
| 154 | TXD/GPB1          | CAP_LED       | O       | L       | GPI        |
| 162 | GPB2              | SCRL_LED      | O       | L       | GPI        |
| 163 | SMCLK0/GPB3       | SMB0_CLK      | SMCLK0  |         | GPI        |
| 164 | SMDAT0/GPB4       | SMB0_DAT      | SMDAT0  |         | GPI        |
| 5   | GA20/GPB5         | A20GATE       | GA20    |         | GPO        |
| 6   | KBRST#/GPB6       | RC_IN#        | KBRST#  |         | KBRST#     |
| 165 | GPB7              | /             | I       |         | GPI        |
| 47  | CLKOUT/GPC0       | /             | O       |         | GPI        |
| 169 | SMCLK1/GPC1       | SMB1_CLK      | SMCLK1  |         | GPI        |
| 170 | SMDAT1/GPC2       | SMB1_DAT      | SMDAT1  |         | GPI        |
| 171 | GPC3              | MAIL_LED      | O       | L       | GPI        |
| 172 | TMR10/WUI2/GPC4   | AC_OK#        | I       |         | GPI        |
| 175 | GPC5              | OP_SD#        | O       | H       | GPI        |
| 176 | TMR11/WUI3/GPC6   | BAT_IN_OC#    | I       | H       | GPI        |
| 1   | CK32KOUT/GPC7     | /             |         |         | GPI        |
| 26  | RI1#/WUI0/GPD0    | SUSB#         | I       |         | GPI        |
| 29  | RI2#/WUI1/GPD1    | SUSC#         | I       |         | GPI        |
| 30  | LPCRST#/WUI4/GPD2 | PLT_RST#      | LPCRST  |         | LPCRST     |
| 31  | ECSCI#/GPD3       | EXT_SCI#      | ECSCI#  | H       | GPI        |
| 41  | GPD4              | RF_ON_SW#     | O       | H       | GPI        |
| 42  | GINT1/GPD5        | /             |         |         | GPI        |
| 62  | TACH0/GPD6        | FAN0_TACH     | TACH0   |         | GPI        |
| 63  | TACH1/GPD7        | /             |         |         | GPI        |
| 87  | ADC4/GPE0         | DISTP_SW#     | I       |         | GPI        |
| 88  | ADC5/GPE1         | /             |         |         | GPI        |
| 89  | ADC6/GPE2         | EMAIL_SW#     | I       |         | GPI        |
| 90  | ADC7/GPE3         | EXPLORE_SW#   | I       |         | GPI        |
| 2   | PWRSW/GPE4        | PWR_SW#       | PWRSW   |         | GPI        |
| 44  | WUI5/GPE5         | /             |         |         | GPI        |
| 24  | LPCPD#/WUI6/GPE6  | LID_EC#       | I       |         | GPI        |
| 25  | CLKRUN#/WUI7/GPE7 | /             |         |         | GPI        |
| 110 | PS2CLK0/GPF0      | /             |         |         | GPI        |
| 111 | PS2DAT0/GPF1      | /             |         |         | GPI        |
| 114 | PS2CLK1/GPF2      | /             |         |         | GPI        |
| 115 | PS2DAT1/GPF3      | /             |         |         | GPI        |
| 116 | PS2CLK2/GPF4      | TP_CLK        | PS2CLK2 |         | GPI        |
| 117 | PS2DAT2/GPF5      | TP_DAT        | PS2DAT2 |         | GPI        |
| 118 | PS2CLK3/GPF6      | /             |         |         | GPI        |
| 119 | PS2DAT3/GPF7      | INTERNET#     | I       |         | GPI        |
| 113 | FA16/GPG0         | FA16          | FA16    |         | GPI        |
| 112 | FA17/GPG1         | FA17          | FA17    |         | GPI        |
| 104 | FA18/GPG2         | FA18          | FA18    |         | GPI        |
| 103 | FA19/GPG3         | /             |         |         | GPI        |
| 3   | FA20/GPG4         | THRM_CPU#     | I       | H       | GPI        |
| 4   | FA21/GPG5         | /             |         |         | GPI        |
| 27  | LPC80HL/GPG6      | PMTHERM#      | O       | H       | GPI        |
| 28  | LPC80LL/GPG7      | AC_APP_UC#    | I       | H       | GPI        |

| Pin | Pin Name | Signal Name | Type | Default |
|-----|----------|-------------|------|---------|
| 48  | GPH0     | VSUS_ON     | O    | L       |
| 54  | GPH1     | VSUS_GD#    | I    | H       |
| 55  | GPH2     | CPUPWR_GD#  | I    | H       |
| 69  | GPH3     | PM_PWRBTN#  | O    | H       |
| 70  | GPH4     | SUSC_ON     | O    | L       |
| 75  | GPH5     | SUSB_ON     | O    | L       |
| 76  | GPH6     | CPU_VRON    | O    | L       |
| 105 | GPH7     | PM_RSMRST#  | O    | L       |
| 148 | GPI0     | ICH7_PWROK  | O    | L       |
| 149 | GPI1     | /           | O    |         |
| 152 | GPI2     | MCHOK       | I    | L       |
| 155 | GPI3     | CHG_EN#     | O    | H       |
| 156 | GPI4     | PRECHG      | O    | L       |
| 168 | GPI5     | BAT_LL#     | O    | H       |
| 174 | GPI6     | BAT_LEARN   | O    | L       |
| 93  | ADC8     | KID0        | I    |         |
| 94  | ADC9     | KID1        | I    |         |
| 101 | DAC2     | BL_PWM_DA   | O    |         |
| 102 | DAC3     | BATSEL_2P#  | O    |         |

| SM-Bus Device   | SM-Bus Address  |
|-----------------|-----------------|
| Clock Generator | 1101001x ( D2 ) |
| SO-DIMM 0       | 1010000x ( A0 ) |
| SO-DIMM 1       | 1010001x ( A2 ) |
| Thermal Sensor  | 01001100 ( 4C ) |
|                 |                 |
|                 |                 |

| PCI Device  | IDSEL# | REQ/GNT# | Interrupts |
|-------------|--------|----------|------------|
| CARD READER | AD17   | 0        | B          |
| 1394        | AD17   | 0        | A          |
| LAN         | AD23   | 2        | C          |

ICH7-M GPIO SETTING

| Pin  | Pin Name            | Signal Name     | Type  | Power Well    | Default |
|------|---------------------|-----------------|-------|---------------|---------|
| AB18 | GPIO00/BI_BSY#      | PM_BMBUSY#      | I     | Core(To:3.3V) | GPI     |
| C8   | GPIO01/REQ5#        | PCI_REQ#5       | I/O   | Core(To:5V)   | GPI     |
| G8   | GPIO02/PIRQE#       | PCI_INTE#       | I(OD) | Core(To:5V)   | GPI     |
| F7   | GPIO03/PIRQF#       | PCI_INTF#       | I(OD) | Core(To:5V)   | GPI     |
| F8   | GPIO04/PIRQG#       | PCI_INTG#       | I(OD) | Core(To:5V)   | GPI     |
| G7   | GPIO05/PIRQH#       | PCI_INTH#       | I(OD) | Core(To:5V)   | GPI     |
| AC21 | GPIO06              | NC              | I/O   | Core(To:3.3V) | GPI     |
| AC18 | GPIO07              | WLAN_BT_LED_EN# |       | Core(To:3.3V) | GPI     |
| E21  | GPIO08              | EXTSM#          | I     | SUS(To:3.3V)  | GPI     |
| E20  | GPIO09              | SATA_DET#0      | I/O   | SUS(To:3.3V)  | GPI     |
| A20  | GPIO10              | WLAN_ON#        | O     | SUS(To:3.3V)  | GPI     |
| B23  | SMBALERT#/GPIO11    | SMB_ALERT#      | I/O   | SUS(To:3.3V)  | Native  |
| F19  | GPIO12              | KBC_SCI#        | I     | SUS(To:3.3V)  | GPI     |
| E19  | GPIO13              | TP              | I/O   | SUS(To:3.3V)  | GPI     |
| R4   | GPIO14              | NC              | I/O   | SUS(To:3.3V)  | GPI     |
| E22  | GPIO15              | CB_SD#          | I/O   | SUS(To:3.3V)  | GPI     |
| AC22 | GPIO16/DPRSLPVR     | PM_DPRSLPVR     | O     | Core(To:3.3V) | Native  |
| D8   | GPIO17/GNT5#        | PCI_GNT#5       | I/O   | Core(To:3.3V) | GPO     |
| AC20 | GPIO18/STP_PCI#     | STP_PCI#        | O     | Core(To:3.3V) | GPO     |
| AH18 | GPIO19/SATA1GP      | NC              | O     | Core(To:3.3V) | GPI     |
| AF21 | GPIO20/STP_CPU#     | STP_CPU#        | O     | Core(To:3.3V) | GPO     |
| AE19 | GPIO21/SATA0GP      | NC              | I/O   | Core(To:3.3V) | GPI     |
| A13  | GPIO22/REQ4#        | PCI_REQ#4       | I/O   | Core(To:3.3V) | Native  |
| AA5  | LDRQ1#/GPIO23       | TP              | I/O   | Core(To:3.3V) | Native  |
| R3   | GPIO24              | NC              | I/O   | SUS(To:3.3V)  | GPO     |
| D20  | GPIO25              | NC              | I/O   | SUS(To:3.3V)  | GPO     |
| A21  | GPIO26/EL_RSVD      | NC              | I/O   | SUS(To:3.3V)  | GPO     |
| B21  | GPIO27/EL_STATE0    | PD_DET#         | I/O   | SUS(To:3.3V)  | GPO     |
| E23  | GPIO28/EL_STATE1    | NC              | I/O   | SUS(To:3.3V)  | GPO     |
| C3   | GPIO29/OC#5         | USB_OC#5        | I/O   | SUS(To:3.3V)  | Native  |
| A2   | GPIO30/OC#6         | NEWCARD_OC#     | I     | SUS(To:3.3V)  | Native  |
| B3   | GPIO31/OC#7         | USB_OC#7        | I/O   | SUS(To:3.3V)  | Native  |
| AG18 | GPIO32/CLKRUN#      | PM_CLKRUN#      | O     | Core(To:3.3V) | GPO     |
| AC19 | GPIO33/AZ_DOCK_EN#  | BT_ON#          | O     | Core(To:3.3V) | GPO     |
| U2   | GPIO34/AZ_DOCK_RST# | NC              | I/O   | Core(To:3.3V) | GPO     |
| AD21 | GPIO35              | NC              | I/O   | Core(To:3.3V) | GPO     |
| AH19 | GPIO36/SATA2GP      | NC              | I/O   | Core(To:3.3V) | GPI     |
| AE19 | GPIO37/SATA3GP      | PCB_ID0         | I     | Core(To:3.3V) | GPI     |
| AD20 | GPIO38              | PCB_ID1         | I     | Core(To:3.3V) | GPI     |
| AE20 | GPIO39              | PCB_ID2         | I     | Core(To:3.3V) | GPI     |
| A14  | GNT4#/GPIO48        | PCI_GNT#4       | I/O   | Core(To:3.3V) | Native  |
| AG24 | GPIO49/CPUPWRGD     | H_PWRGD         | O     | V_CPU_IO      | Native  |

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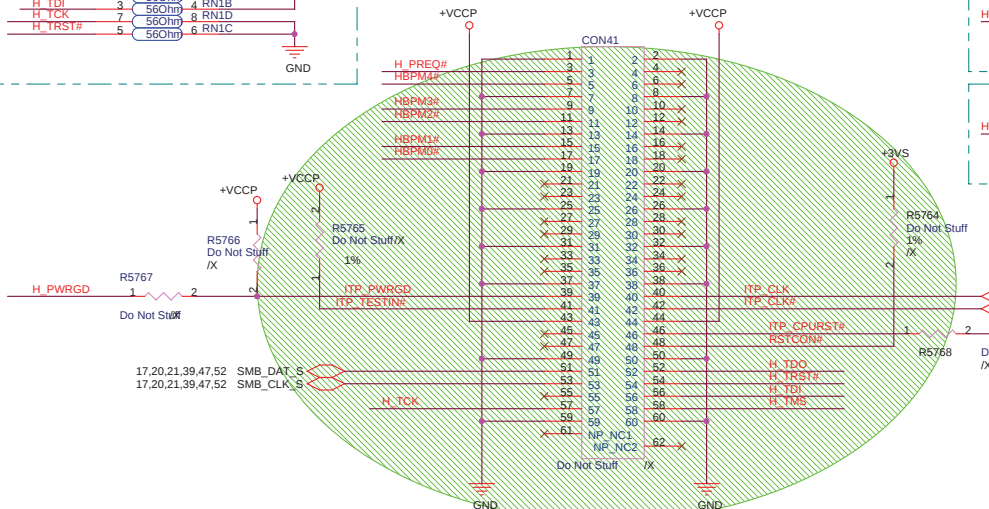
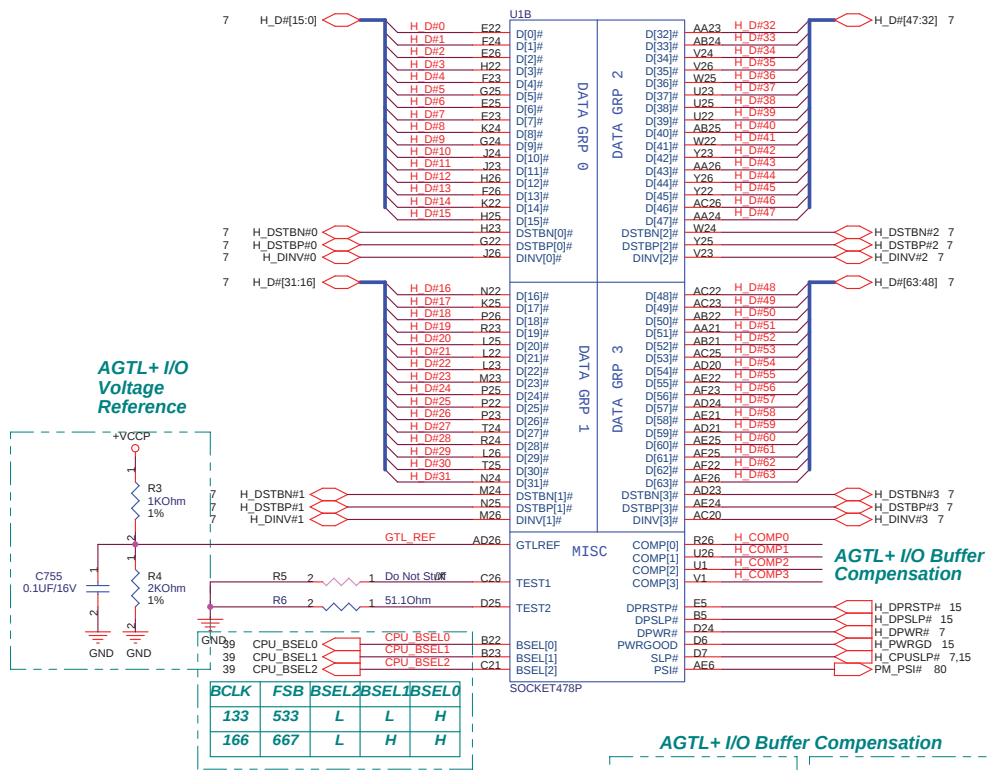
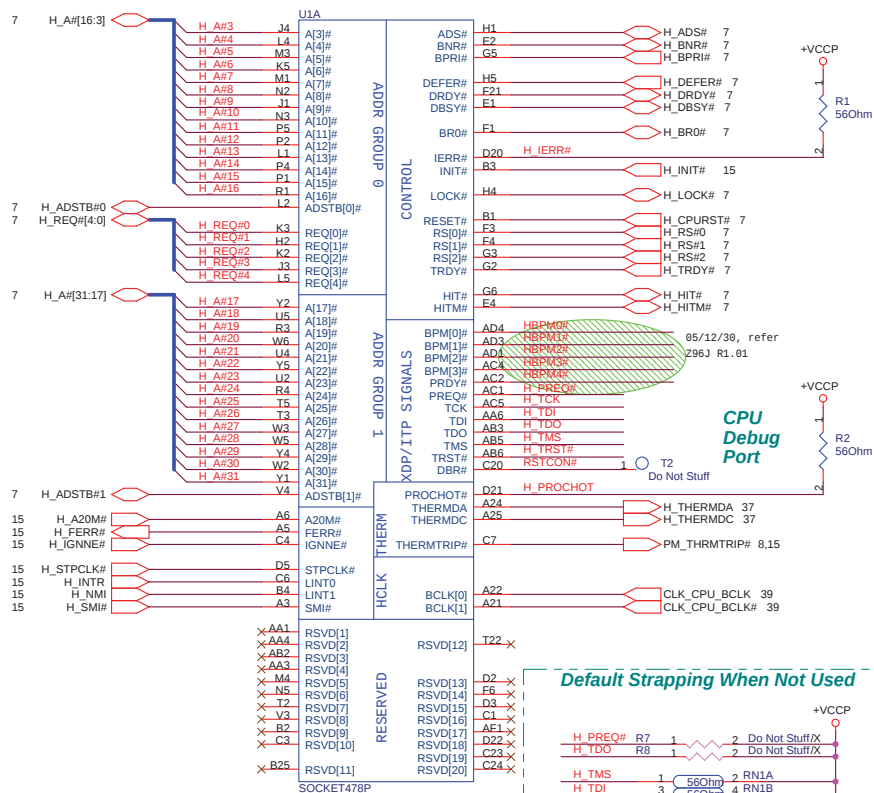
ASUSTek Computer INC. Engineer: Mike Lee

Size Custom

Project Name S96F

Rev 2.0G

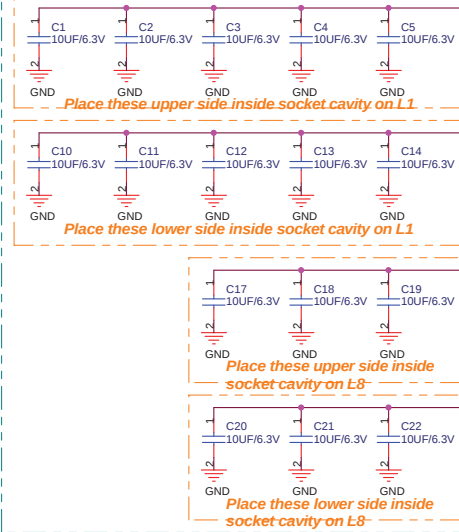
Date: Friday, April 07, 2006 Sheet 2 of 96



0407\_1445

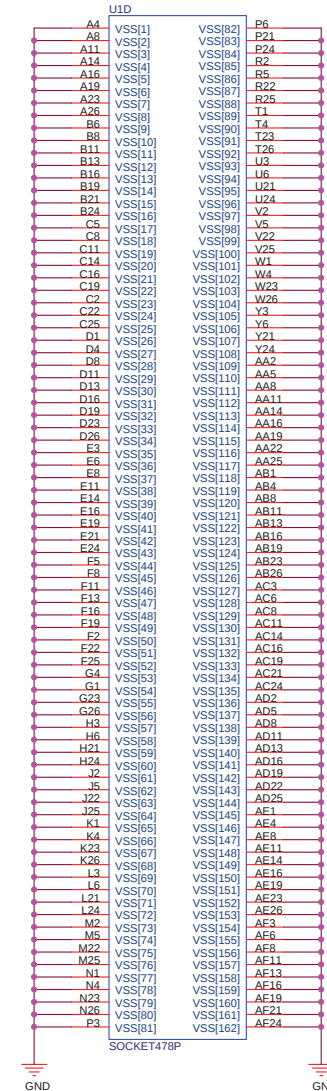
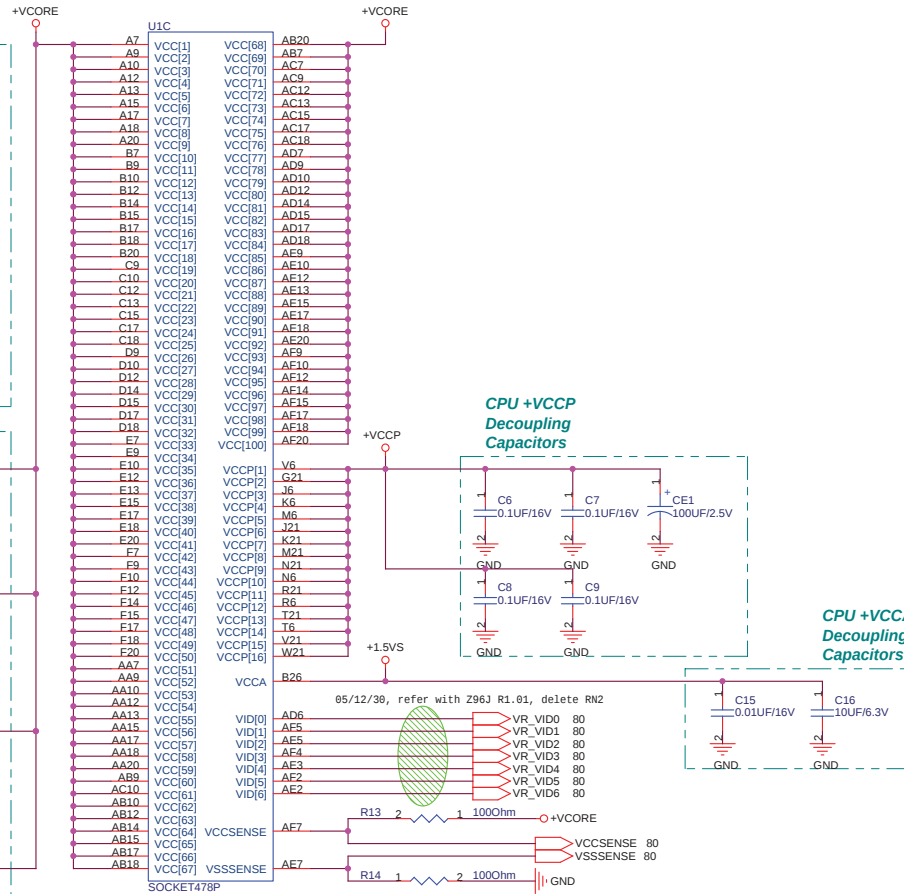
**CPU +VCORE  
Bulk-Decoupling  
Capacitors**

**CPU +VCORE  
Mid-Frequency  
Capacitors**



**+VCORE Mid-Frequency Capacitor**  
Intel: 22UF \*32  
R1F: 10UF \*16

**+VCCP Decoupling Capacitor**  
Intel: 270UF \*1, 0.1UF \*6  
R1F: 220UF \*1, 0.1UF \*4



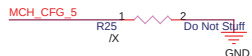
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## GMCH Strapping

### CFG5 : DMI Strap

0 = DMI x2  
1 = DMI x4 (D)

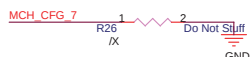


### CFG[13:12] : GMCH Test Mode

00 = Partial CLK Gating Disable  
01 = XOR Mode Enable  
10 = All Z Mode Enable  
11 = Normal Operation (D)

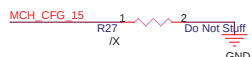
### CFG7 : CPU Strap

0 = DT/Transpotable CPU  
1 = Mobile CPU (D)



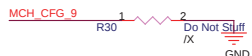
### CFG15 : ICH RESET Disable

0 = ICH Reset Disable  
1 = Normal Operation (D)



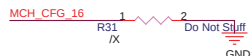
### CFG9 : PCIE Graphic Lane

0 = Reverse Lane  
1 = Normal Operation (D)



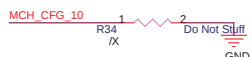
### CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable  
1 = Dynamic ODT Enable (D)



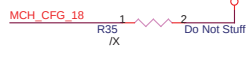
### CFG10 : HOST PLL VCO Select

0 = Reserved  
1 = Mobility (D)



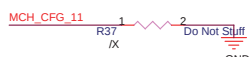
### CFG18 : VCC Select

0 = 1.05V (D)  
1 = 1.5V



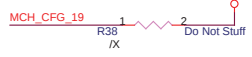
### CFG11 : PSB 4x CLK Enable

0 = 4x Enable  
1 = 8x Enable (D)



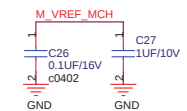
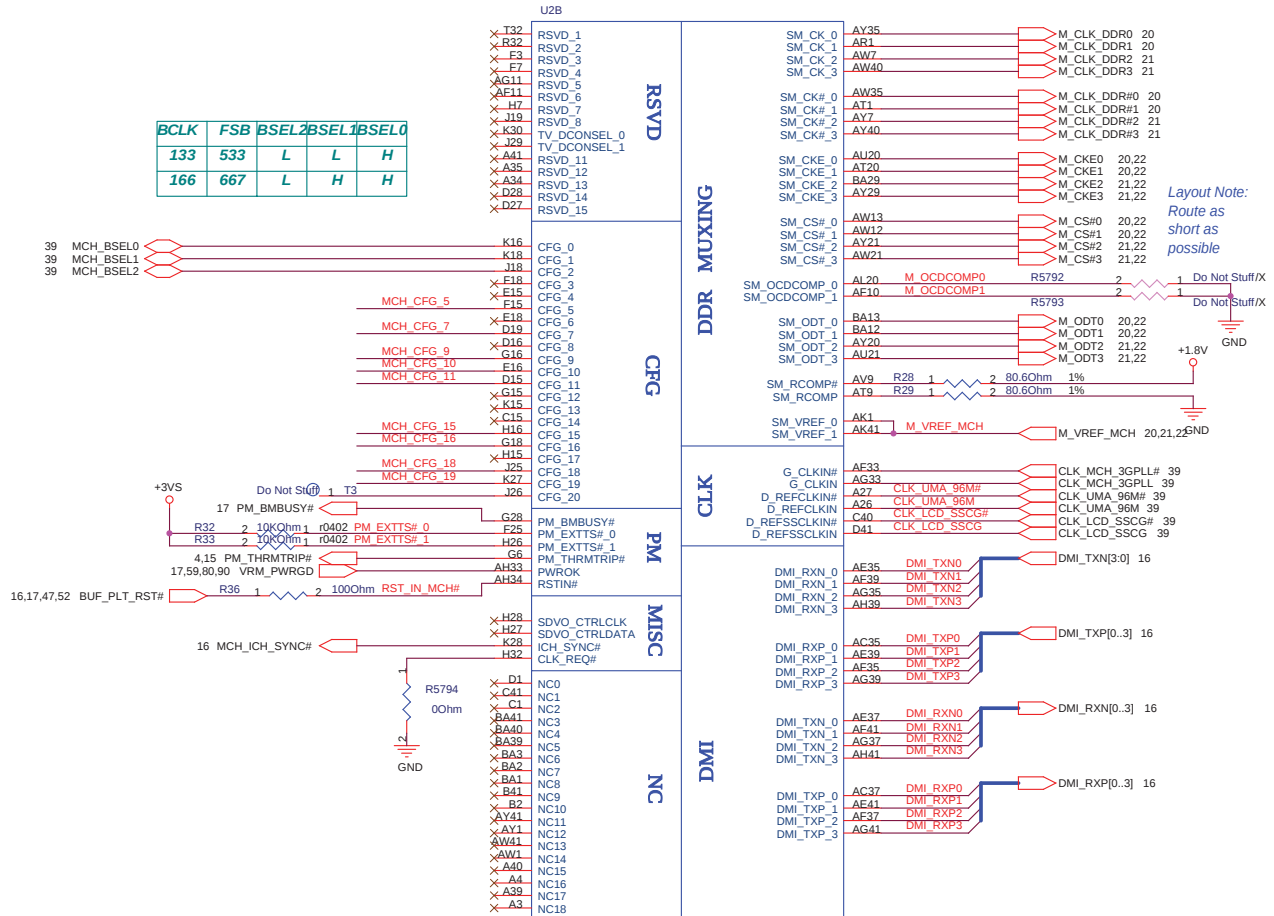
### CFG19 : DMI Lane Reversal

0 = Normal Operation (D)  
1 = Lanes Reversed

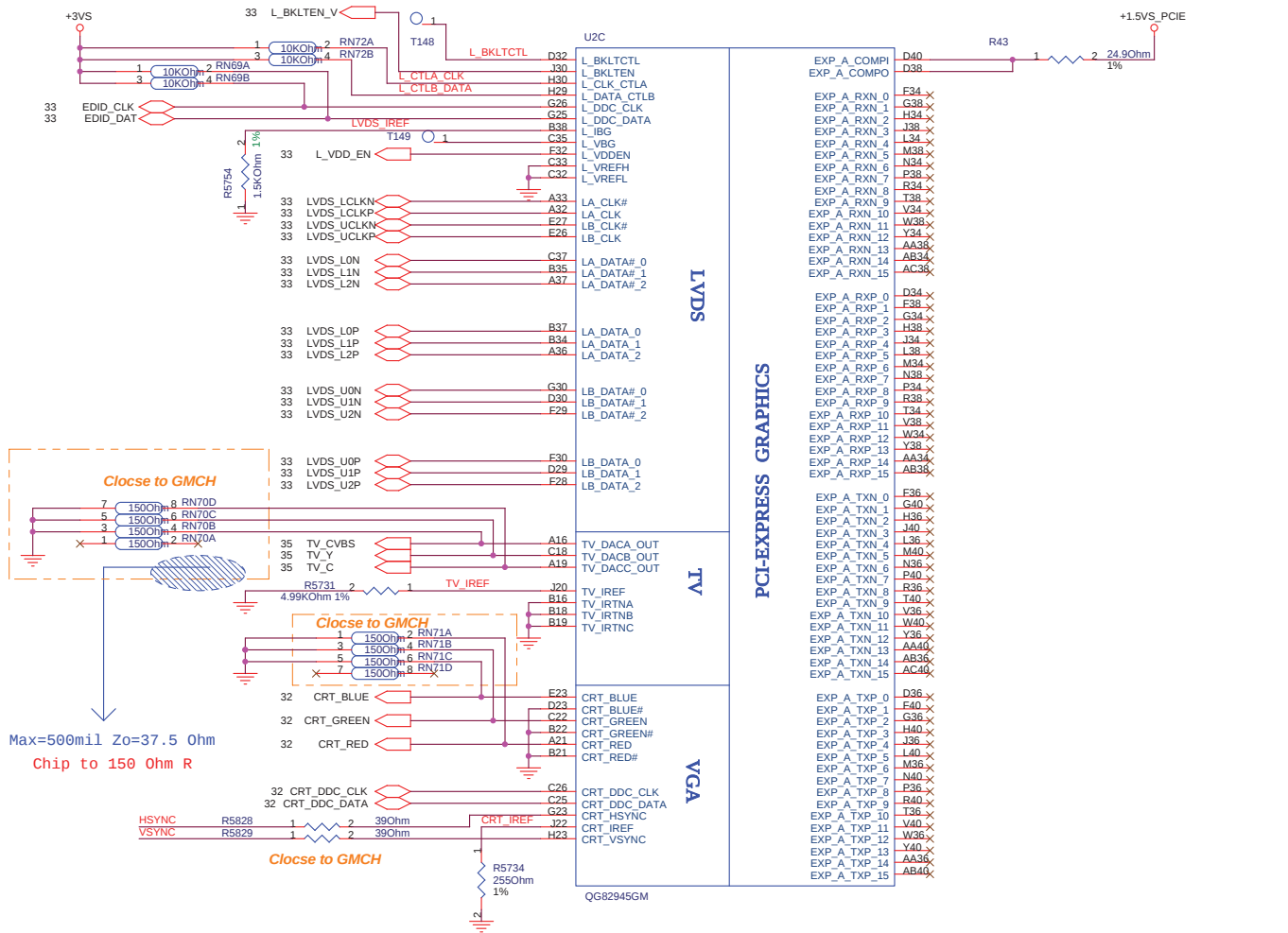


Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

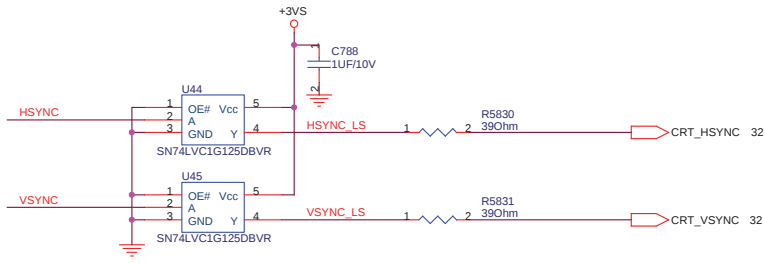
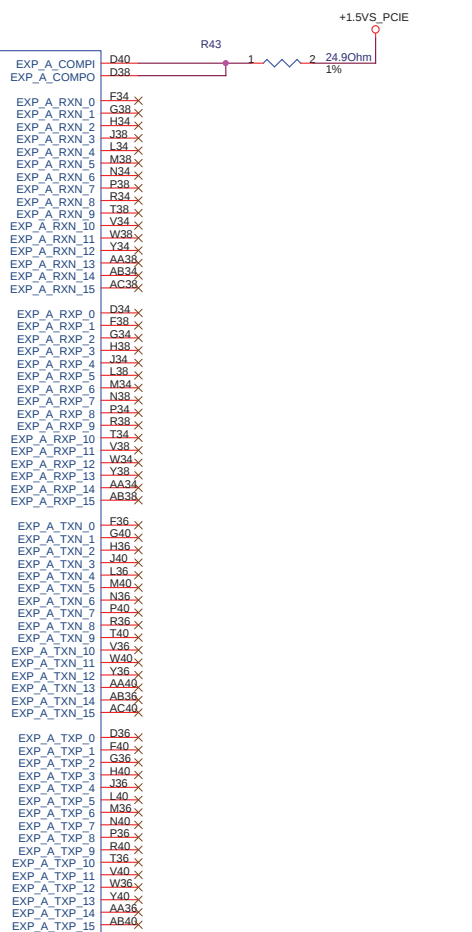
| BCLK | FSB | BSEL2 | BSEL1 | BSEL0 |
|------|-----|-------|-------|-------|
| 133  | 533 | L     | L     | H     |
| 166  | 667 | L     | H     | H     |



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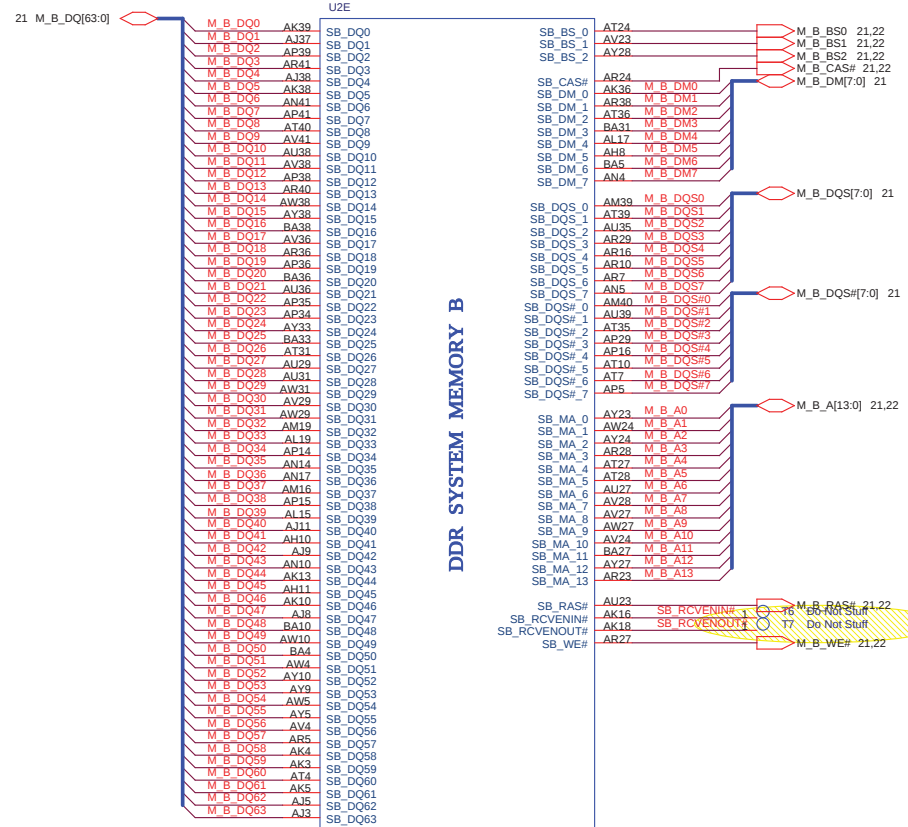
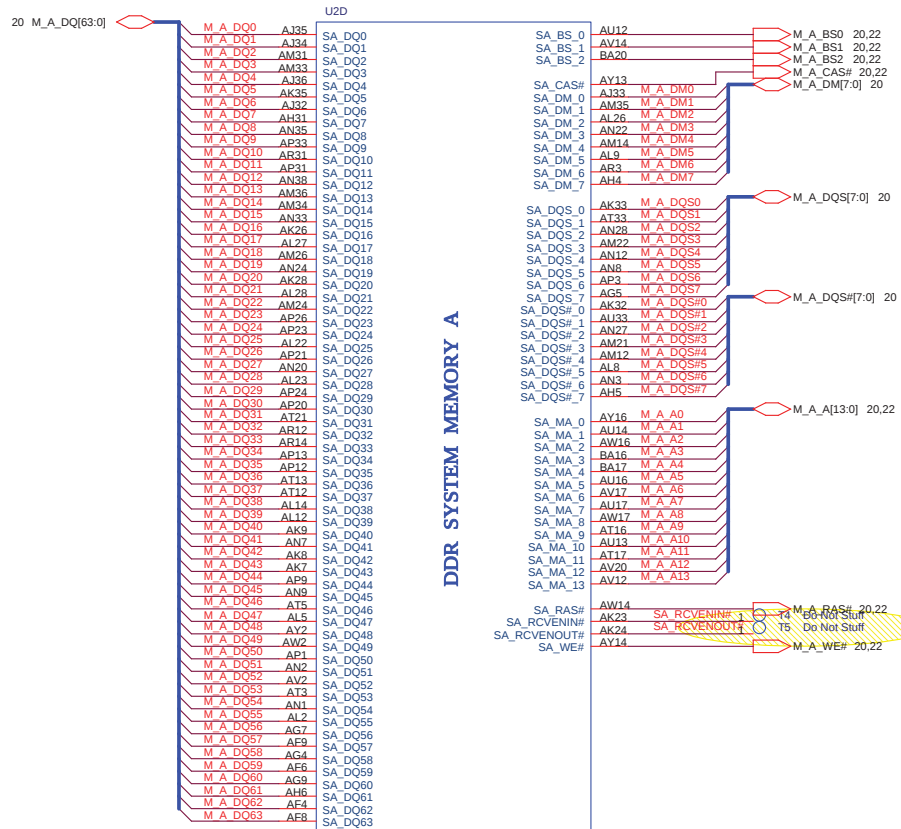


# PCI-EXPRESS GRAPHICS

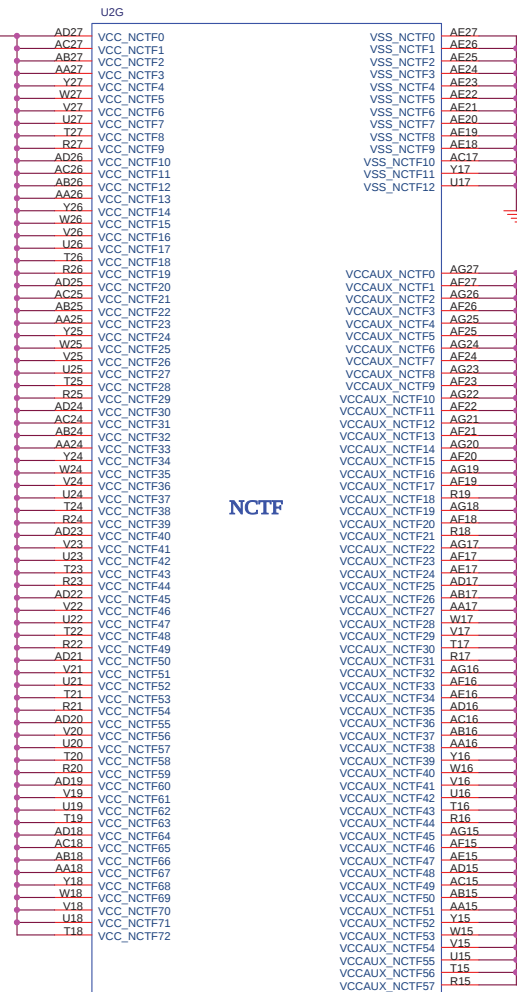
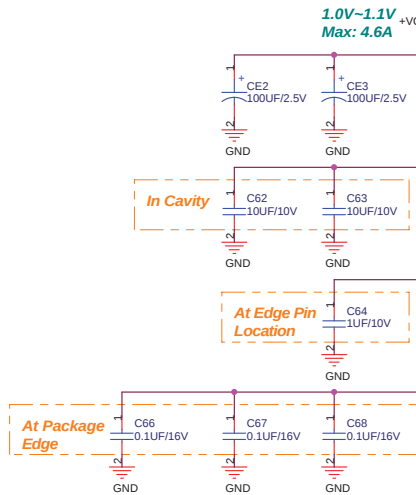
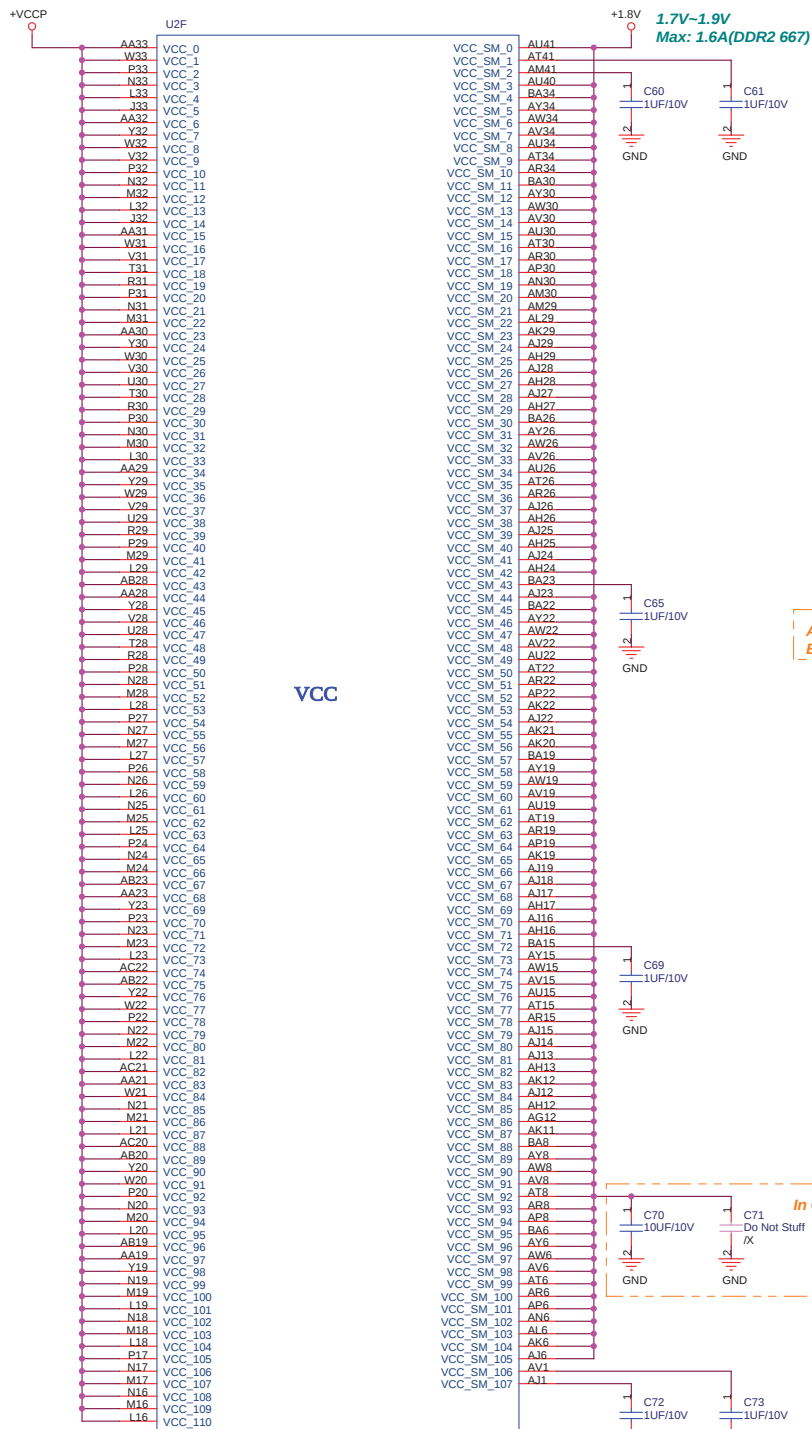


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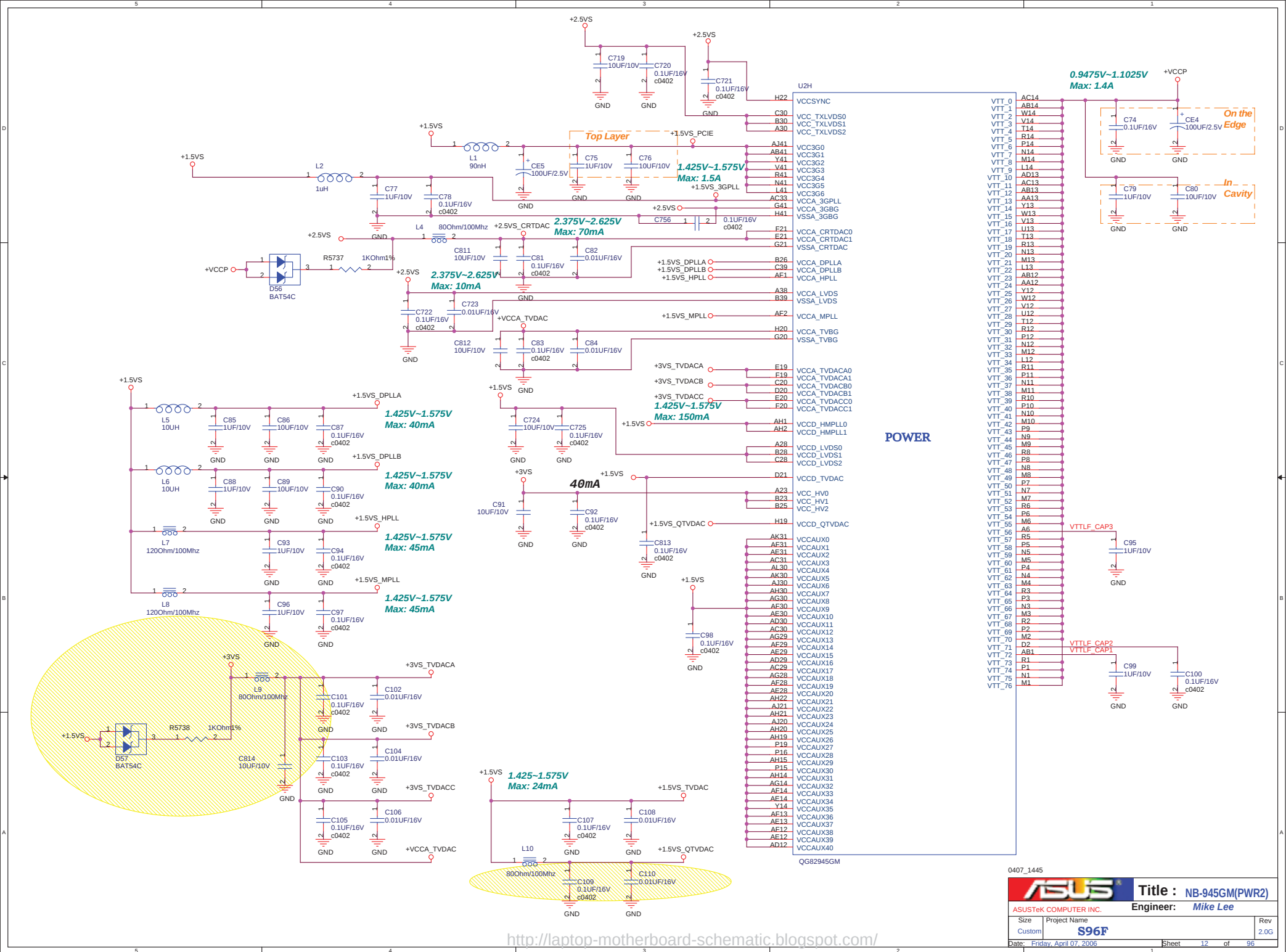
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|------------------------------|--------------|----------------------------------|-------|
| <b>ASUS</b>                  |              | <b>Title : NB-945GM(GRAPHIC)</b> |       |
| ASUSTek COMPUTER INC.        |              | Engineer: <b>Mike Lee</b>        |       |
| Size                         | Project Name | Rev                              |       |
| Custom                       | <b>S96F</b>  | 2.0G                             |       |
| Date: Friday, April 07, 2006 | Sheet        | 9                                | of 96 |

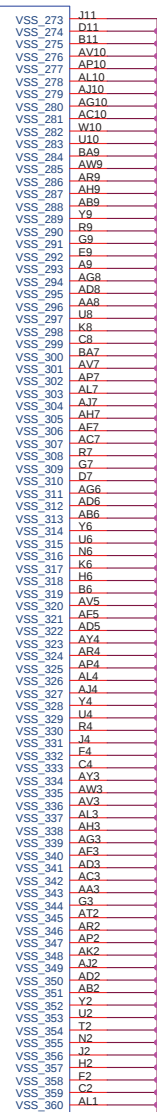
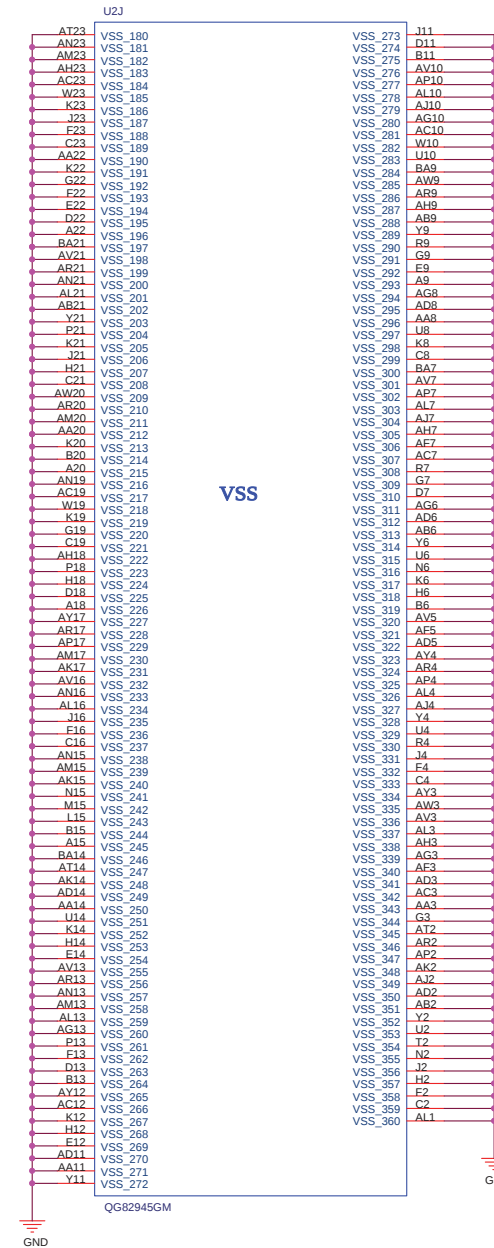
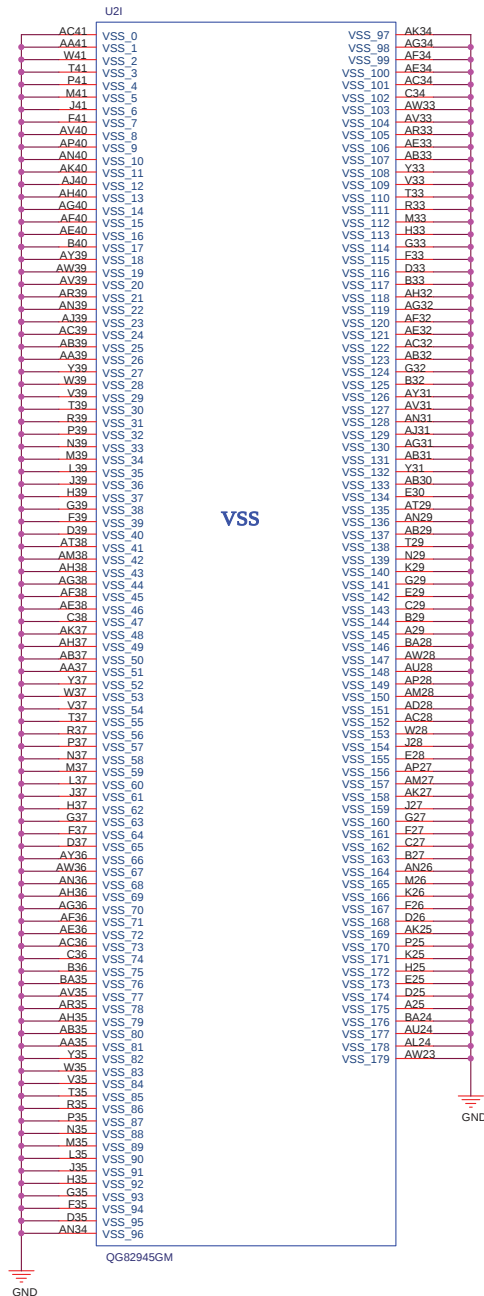


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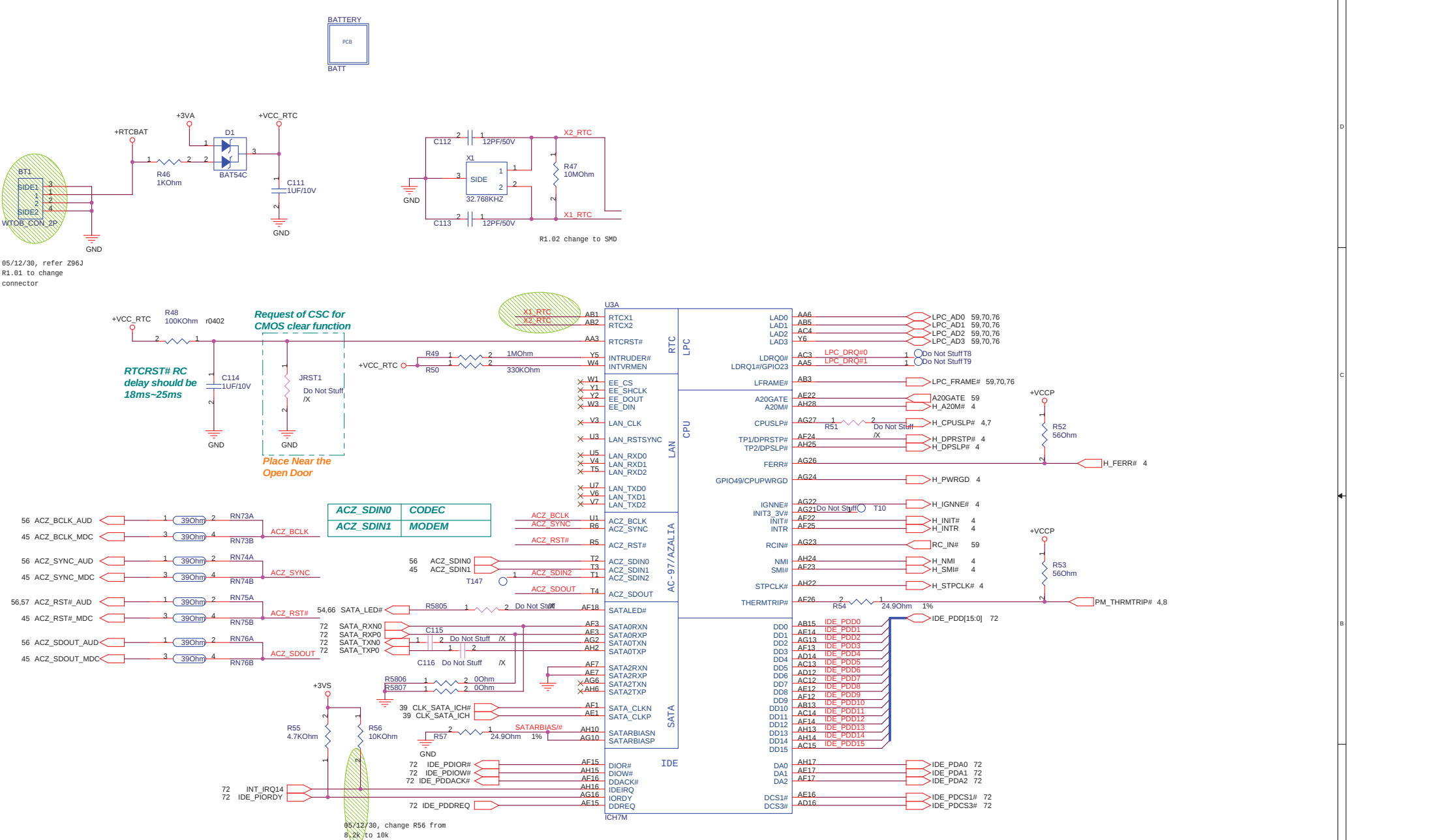
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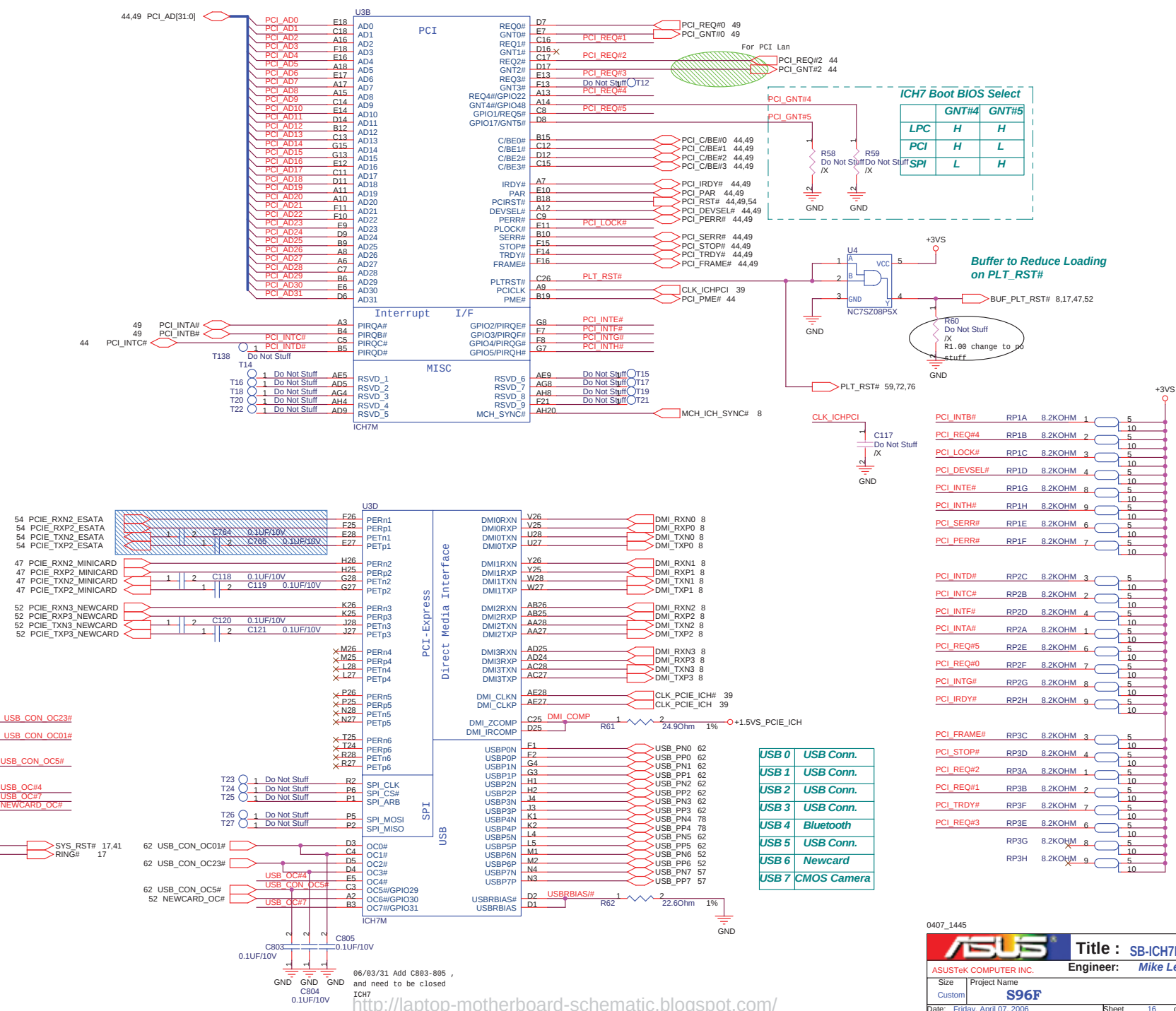


0407\_1445

|                              |              |                       |       |
|------------------------------|--------------|-----------------------|-------|
| <b>ASUS</b>                  |              | Title : NB-945PM(GND) |       |
| ASUSTeK COMPUTER INC.        |              | Engineer: Mike Lee    |       |
| Size                         | Project Name | Rev                   |       |
| Custom                       | S96F         | 2.0G                  |       |
| Date: Friday, April 07, 2006 | Sheet        | 13                    | of 96 |



0407\_1445



ICH7 Boot BIOS Select

|     | GNT#4 | GNT#5 |
|-----|-------|-------|
| LPC | H     | H     |
| PCI | H     | L     |
| SPI | L     | H     |

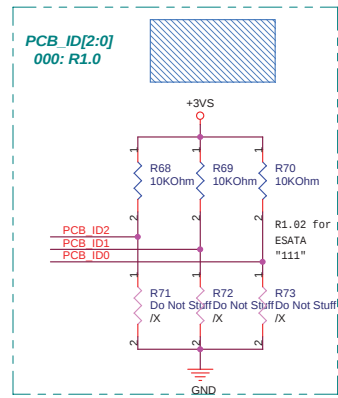
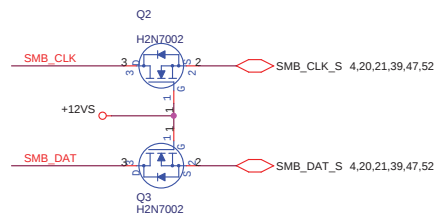
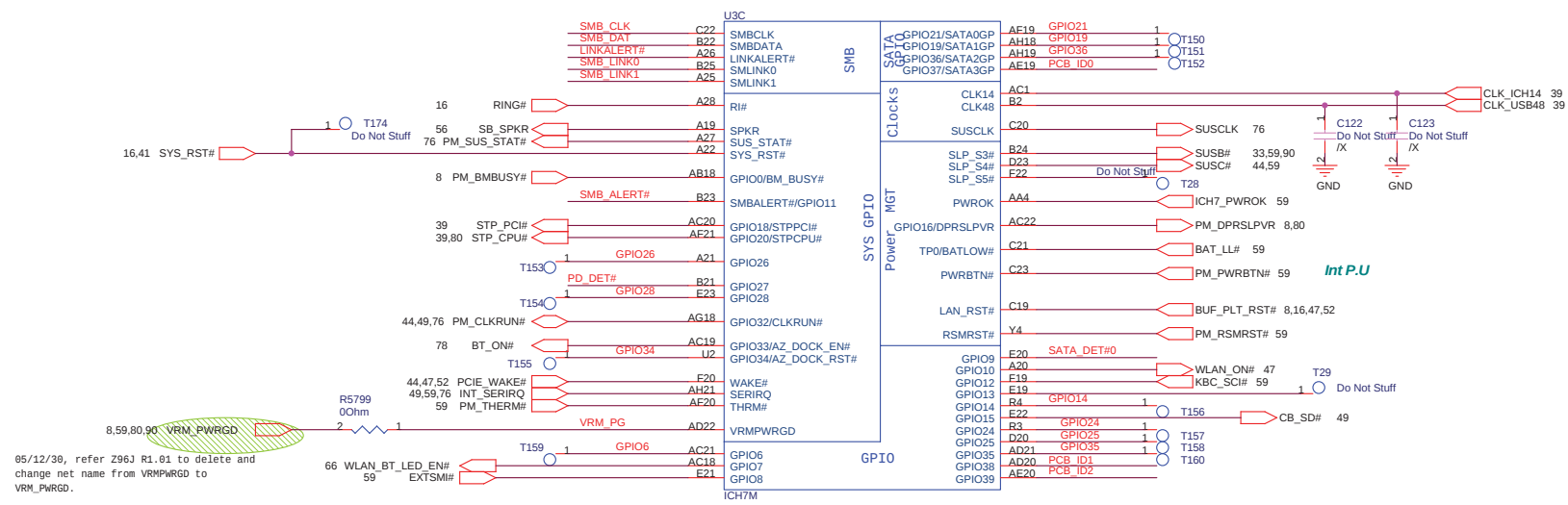
Buffer to Reduce Loading on PLT\_RST#

|             |      |         |   |    |
|-------------|------|---------|---|----|
| PCI_INTB#   | RP1A | 8.2KOHM | 1 | 5  |
| PCI_REQ#4   | RP1B | 8.2KOHM | 2 | 10 |
| PCI_LOCK#   | RP1C | 8.2KOHM | 3 | 10 |
| PCI_DEVSEL# | RP1D | 8.2KOHM | 4 | 5  |
| PCI_INTE#   | RP1G | 8.2KOHM | 8 | 10 |
| PCI_INTH#   | RP1H | 8.2KOHM | 9 | 10 |
| PCI_SERR#   | RP1E | 8.2KOHM | 6 | 10 |
| PCI_PERR#   | RP1F | 8.2KOHM | 7 | 10 |

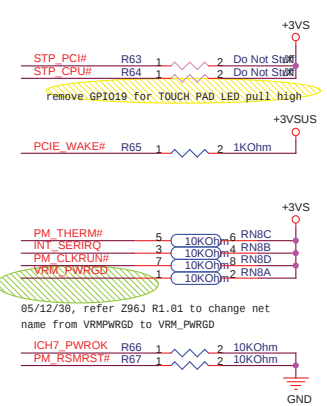
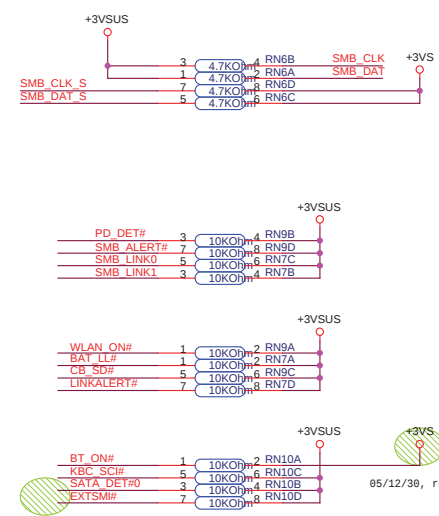
|           |      |         |   |    |
|-----------|------|---------|---|----|
| PCI_INTD# | RP2C | 8.2KOHM | 3 | 5  |
| PCI_INTC# | RP2B | 8.2KOHM | 2 | 10 |
| PCI_INTF# | RP2D | 8.2KOHM | 4 | 10 |
| PCI_INTA# | RP2A | 8.2KOHM | 1 | 5  |
| PCI_REQ#5 | RP2E | 8.2KOHM | 6 | 5  |
| PCI_REQ#0 | RP2F | 8.2KOHM | 7 | 5  |
| PCI_INTG# | RP2G | 8.2KOHM | 8 | 5  |
| PCI_IRDY# | RP2H | 8.2KOHM | 9 | 10 |

|            |      |         |   |    |
|------------|------|---------|---|----|
| PCI_FRAME# | RP3C | 8.2KOHM | 3 | 5  |
| PCI_STOP#  | RP3D | 8.2KOHM | 4 | 5  |
| PCI_REQ#2  | RP3A | 8.2KOHM | 1 | 10 |
| PCI_REQ#1  | RP3B | 8.2KOHM | 2 | 5  |
| PCI_TRDY#  | RP3F | 8.2KOHM | 7 | 5  |
| PCI_REQ#3  | RP3E | 8.2KOHM | 6 | 5  |
|            | RP3G | 8.2KOHM | 8 | 5  |
|            | RP3H | 8.2KOHM | 9 | 5  |

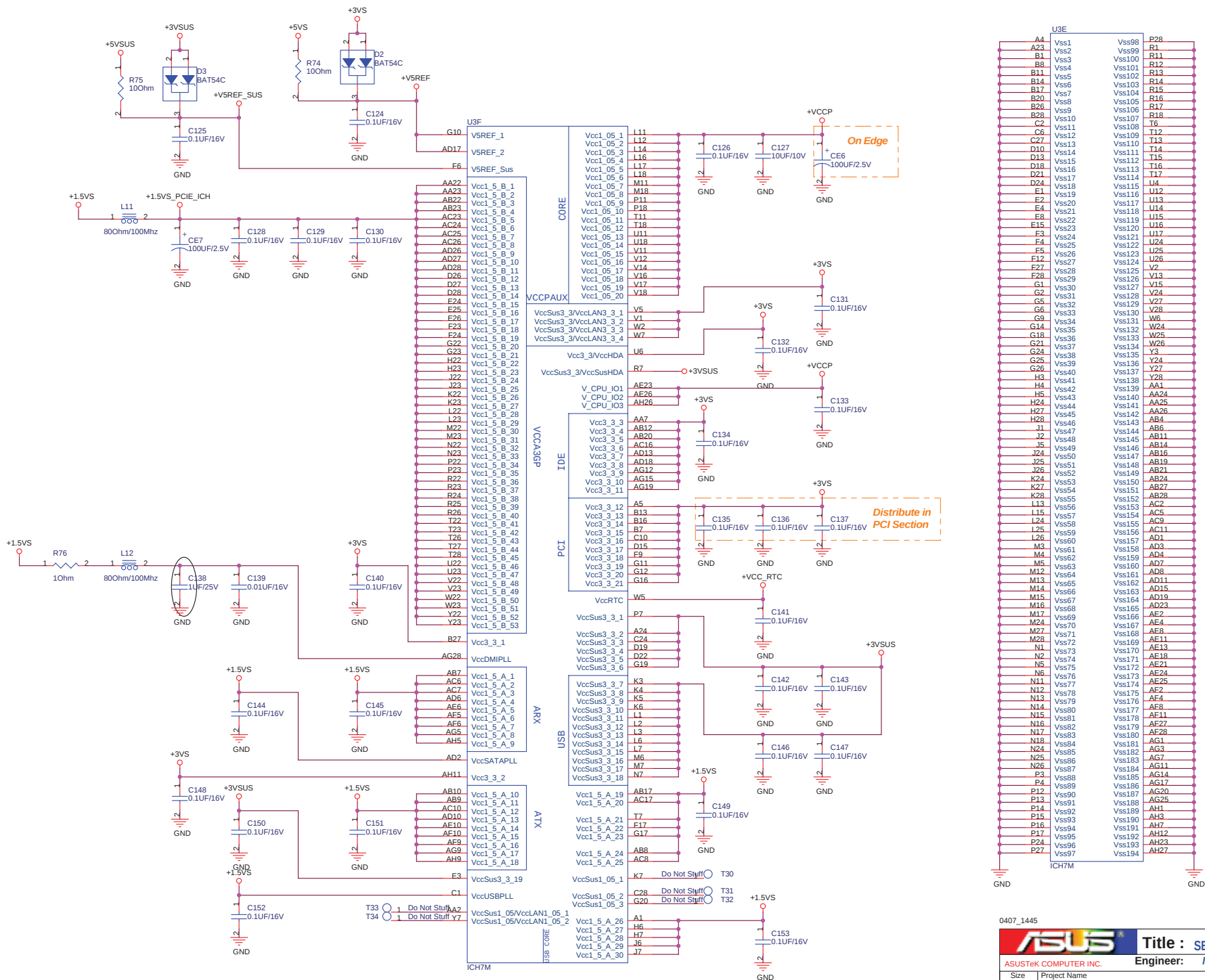
| USB 0 | USB Conn.   |
|-------|-------------|
| USB 1 | USB Conn.   |
| USB 2 | USB Conn.   |
| USB 3 | USB Conn.   |
| USB 4 | Bluetooth   |
| USB 5 | USB Conn.   |
| USB 6 | Newcard     |
| USB 7 | CMOS Camera |



PCB\_VID3 : PROJECT CODE



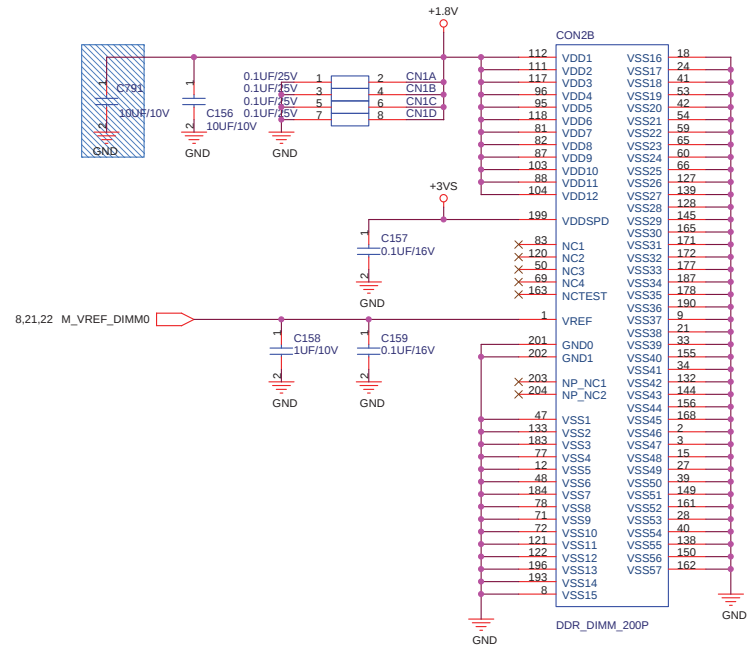
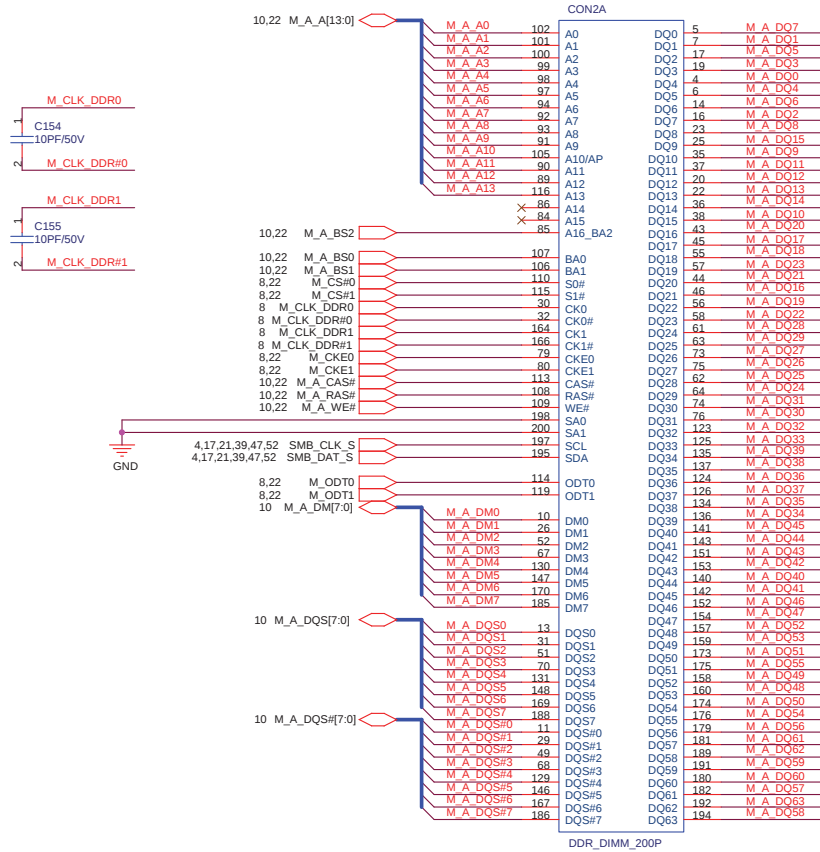
0407\_1445



0407\_1445

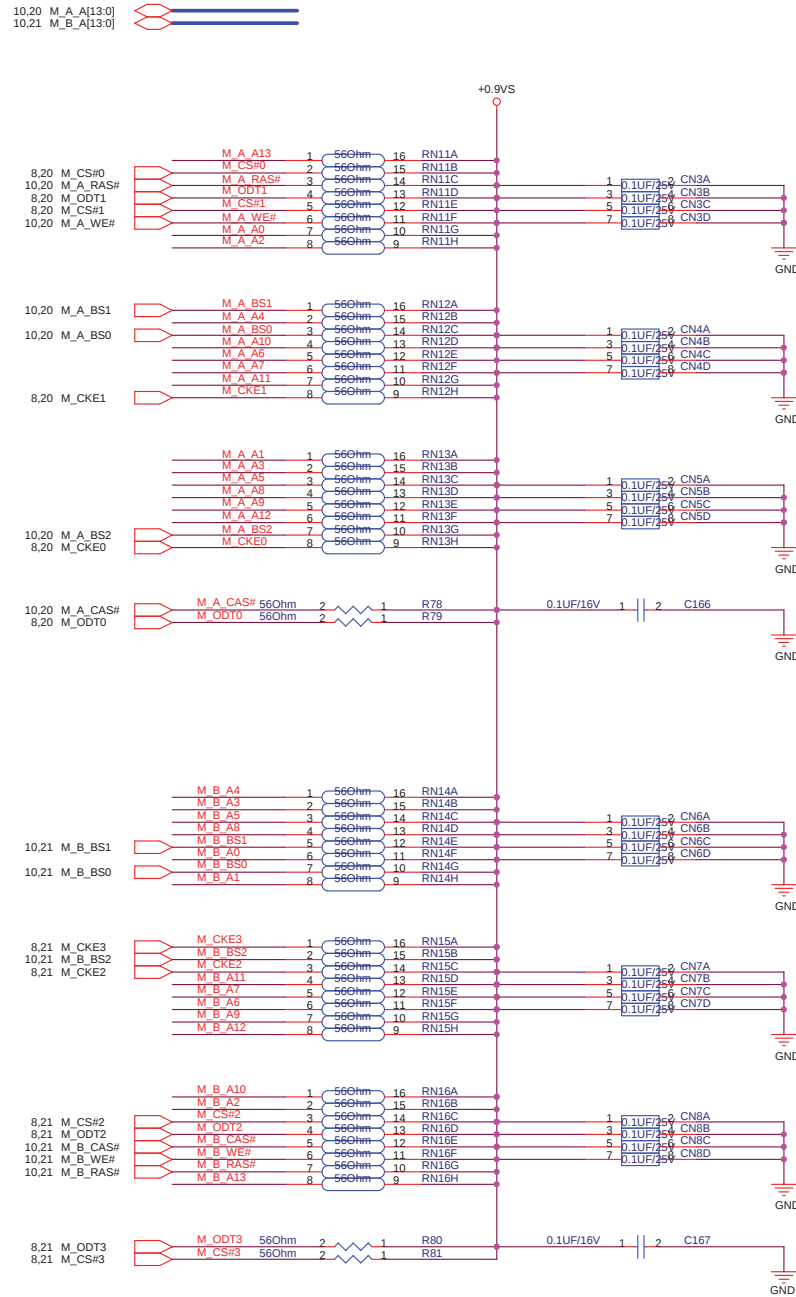
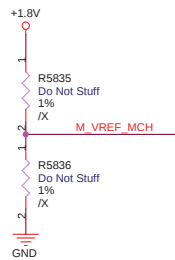
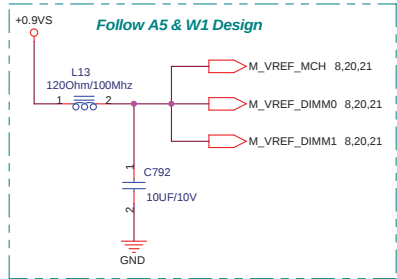
M\_A\_DQ[63:0] 10

REV Type

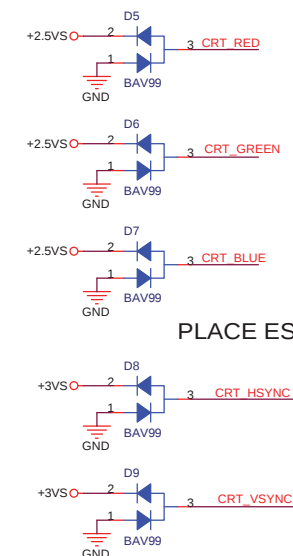
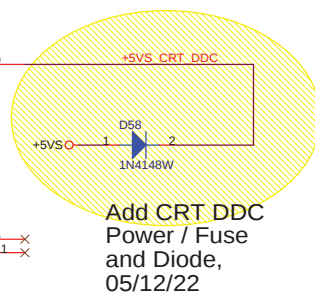
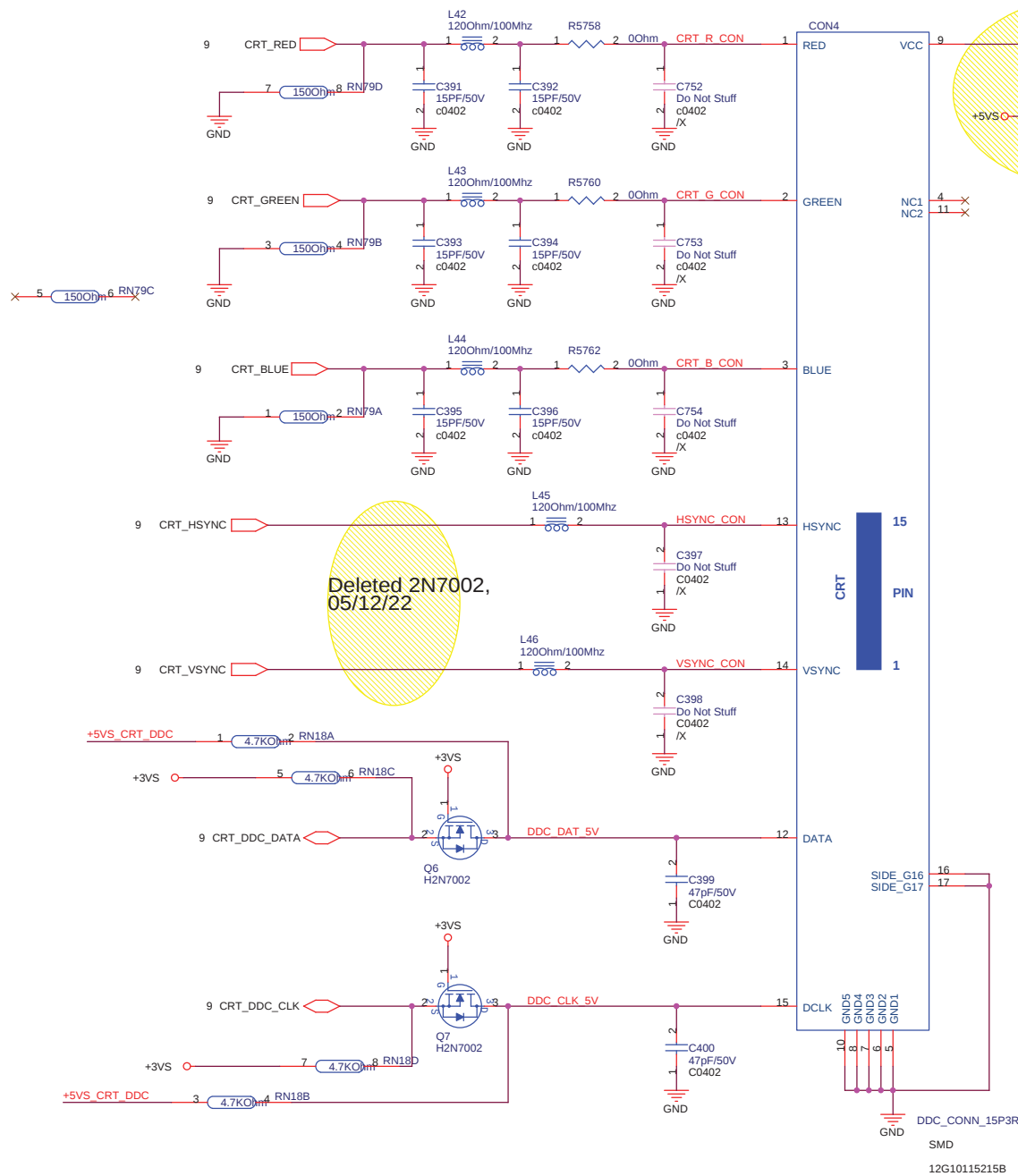


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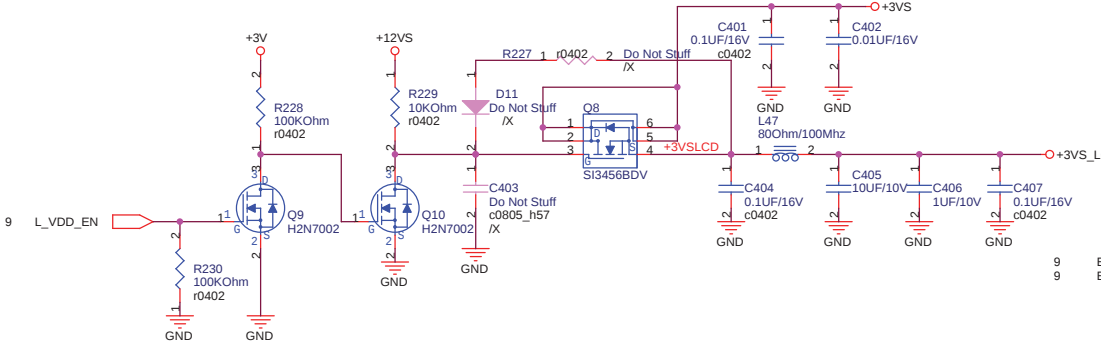
0407\_1445



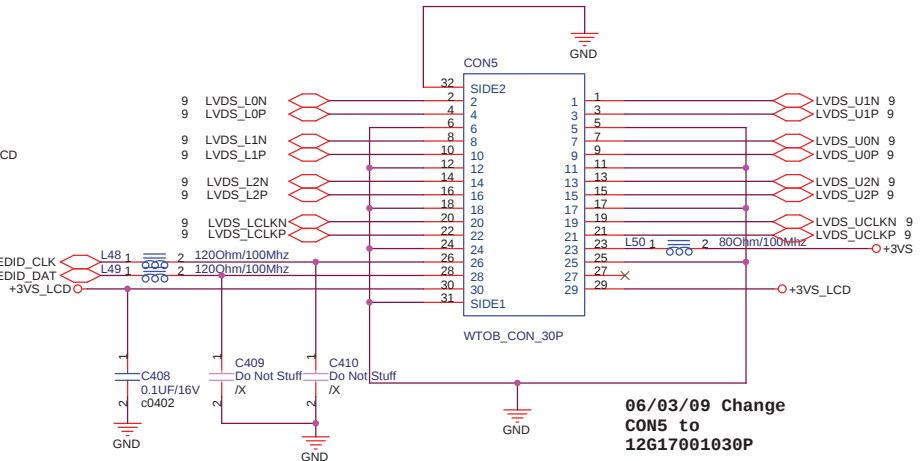
06/03/03 change HSYNC/VSYNC ESD power rail from +5v to +3v

# LCD Backlight Control

## LCD Power

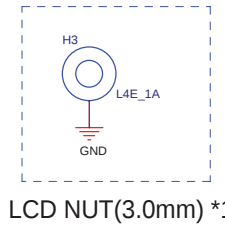
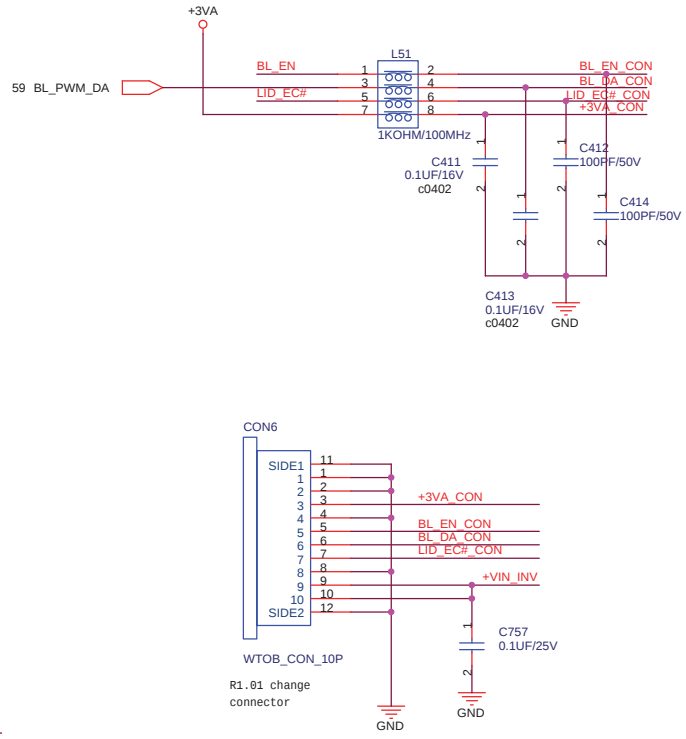
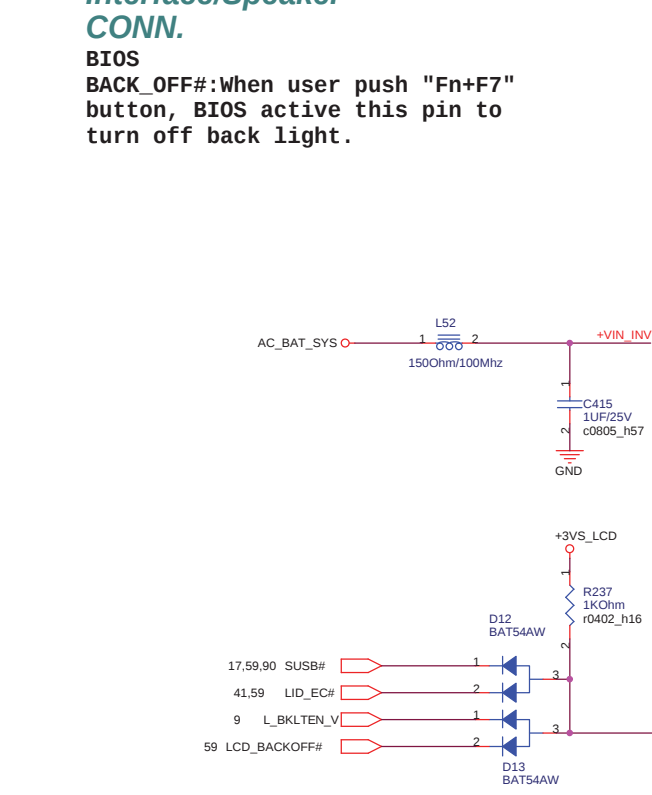


# LCD LVDS Interface



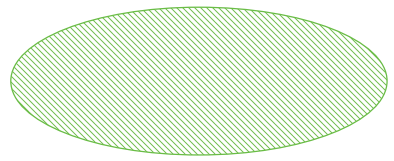
## INVERTER Interface/Speaker CONN.

BIOS  
BACK\_OFF#:When user push "Fn+F7"  
button, BIOS active this pin to  
turn off back light.

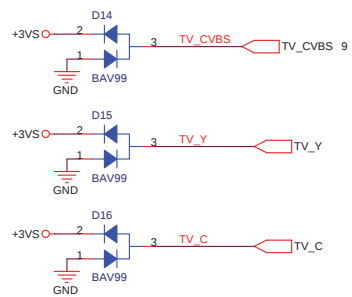


LCD NUT(3.0mm) \*1

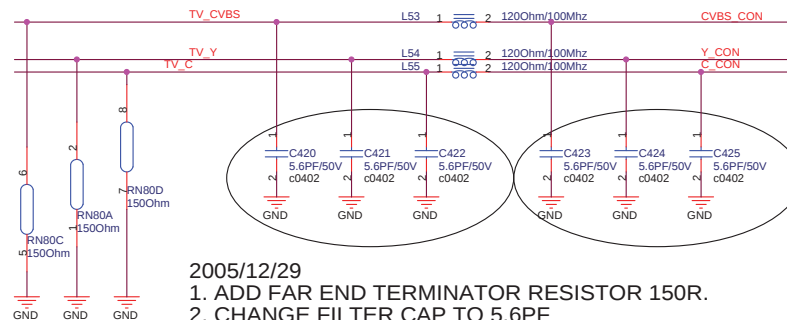
05/12/30 refer Z96J R1.01 to  
remove HW pannel ID setting



# TV OUT

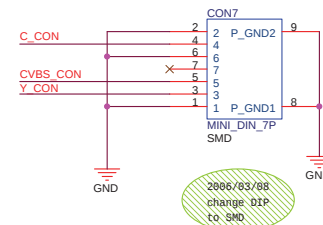


PLACE ESD Diodes near TV port

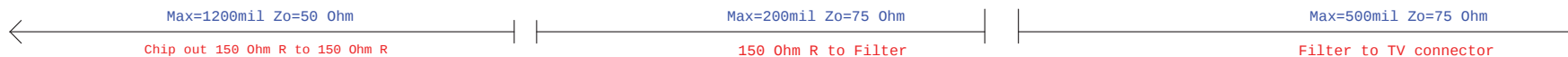


2005/12/29

1. ADD FAR END TERMINATOR RESISTOR 150R.
2. CHANGE FILTER CAP TO 5.6PF



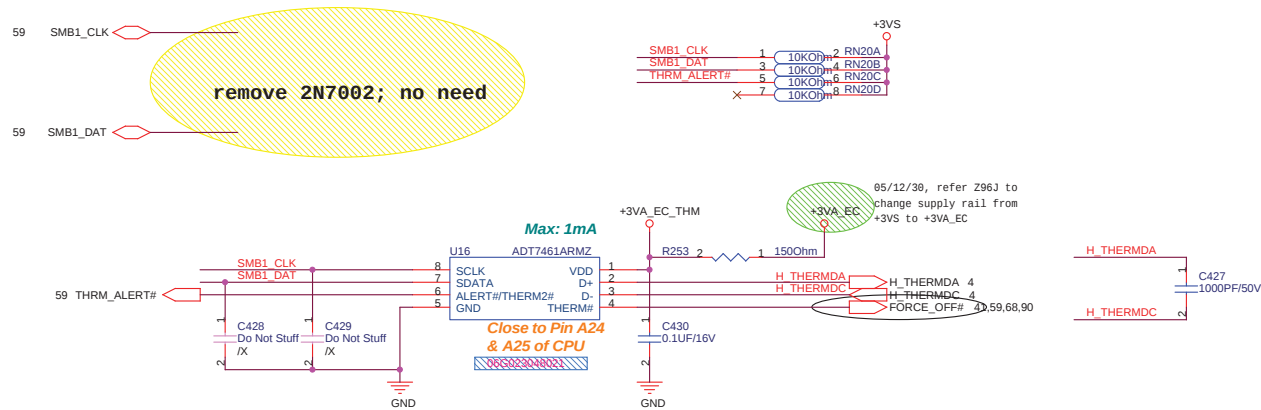
2006/03/08  
change DIP to SMD



0407\_1445

|                              |              |                                      |          |
|------------------------------|--------------|--------------------------------------|----------|
| <b>ASUS</b>                  |              | <b>Title : TV OUT &amp; DVI CON.</b> |          |
| ASUSTek COMPUTER INC         |              | Engineer: <b>Mike Lee</b>            |          |
| Size                         | Project Name | Rev                                  |          |
| Custom                       | <b>S96F</b>  | <b>2.0G</b>                          |          |
| Date: Friday, April 07, 2006 |              | Sheet                                | 35 of 96 |

## Thermal Sensor



Route H\_THERMDA and H\_THERMDC on the same layer

-----OTHER SIGNALS

15 mils

=====GND

10 mils

=====H\_THERMDA(10 mils)

10 mils

=====H\_THERMDC(10 mils)

10 mils

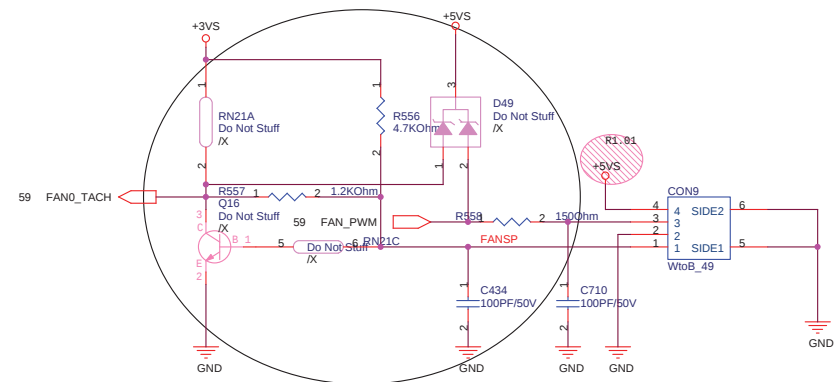
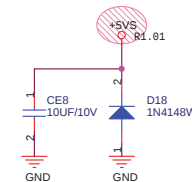
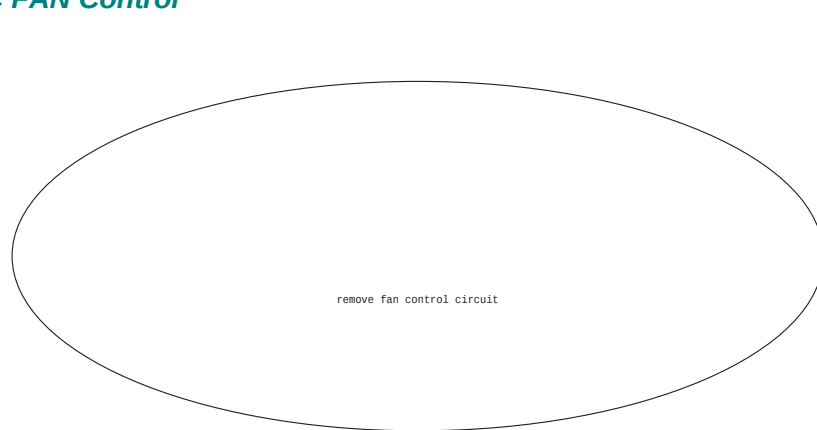
=====GND

15 mils

-----OTHER SIGNALS

Avoid FSB,Power

## DC FAN Control

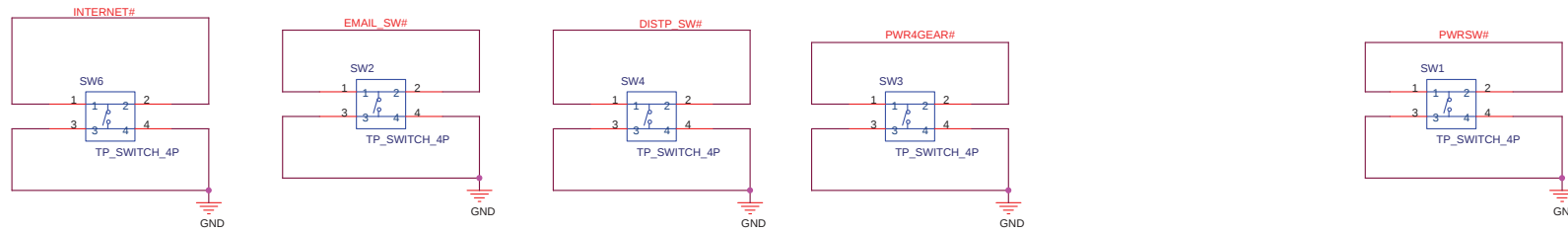


CPU FAN will be forced on:  
1) Thermal Sensor Over-temperature  
2) WATCHDOG asserted by EC

0407\_1445

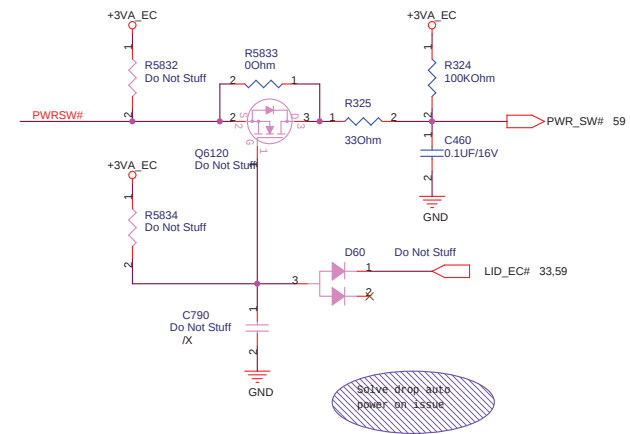
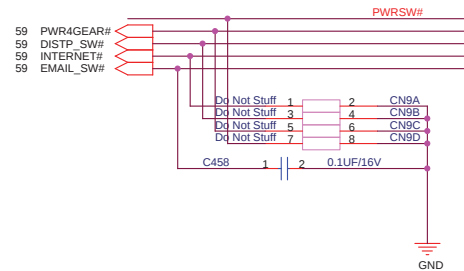
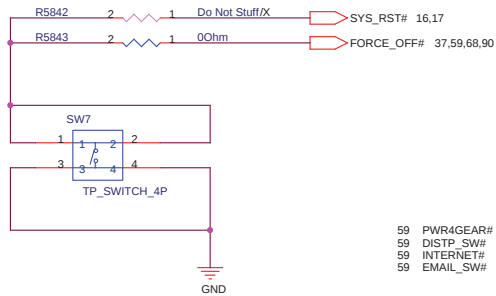
|                              |              |                           |       |
|------------------------------|--------------|---------------------------|-------|
| <b>ASUS</b>                  |              | Title : THER SENSOR & FAN |       |
| ASUSTek COMPUTER INC.        |              | Engineer: Mike Lee        |       |
| Size                         | Project Name | Rev                       |       |
| Custom                       | S96F         | 2.0G                      |       |
| Date: Friday, April 07, 2006 | Sheet        | 37                        | of 96 |



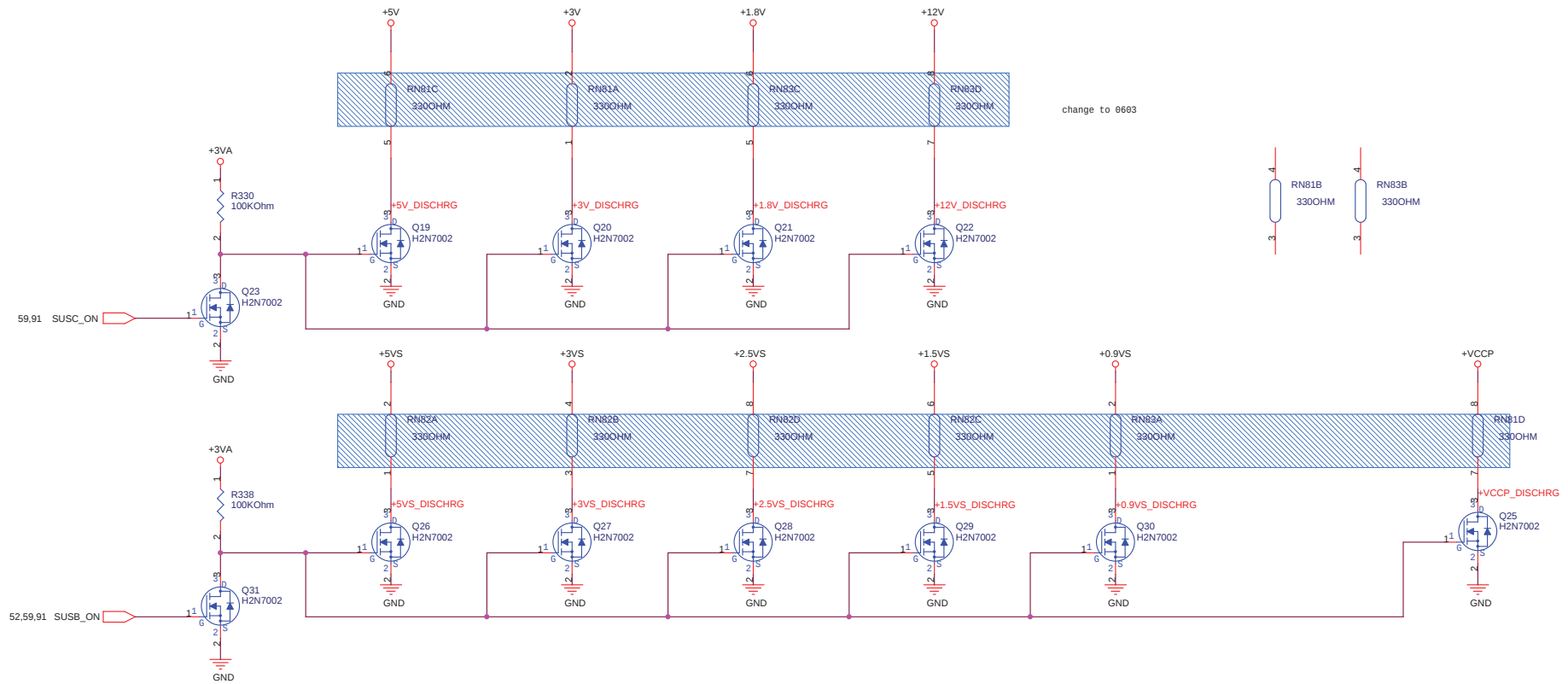


06/03/09 Change  
SW1-4, SW6-7 to  
12G09103004P

SHUT\_DOWN#  
/ RESET#

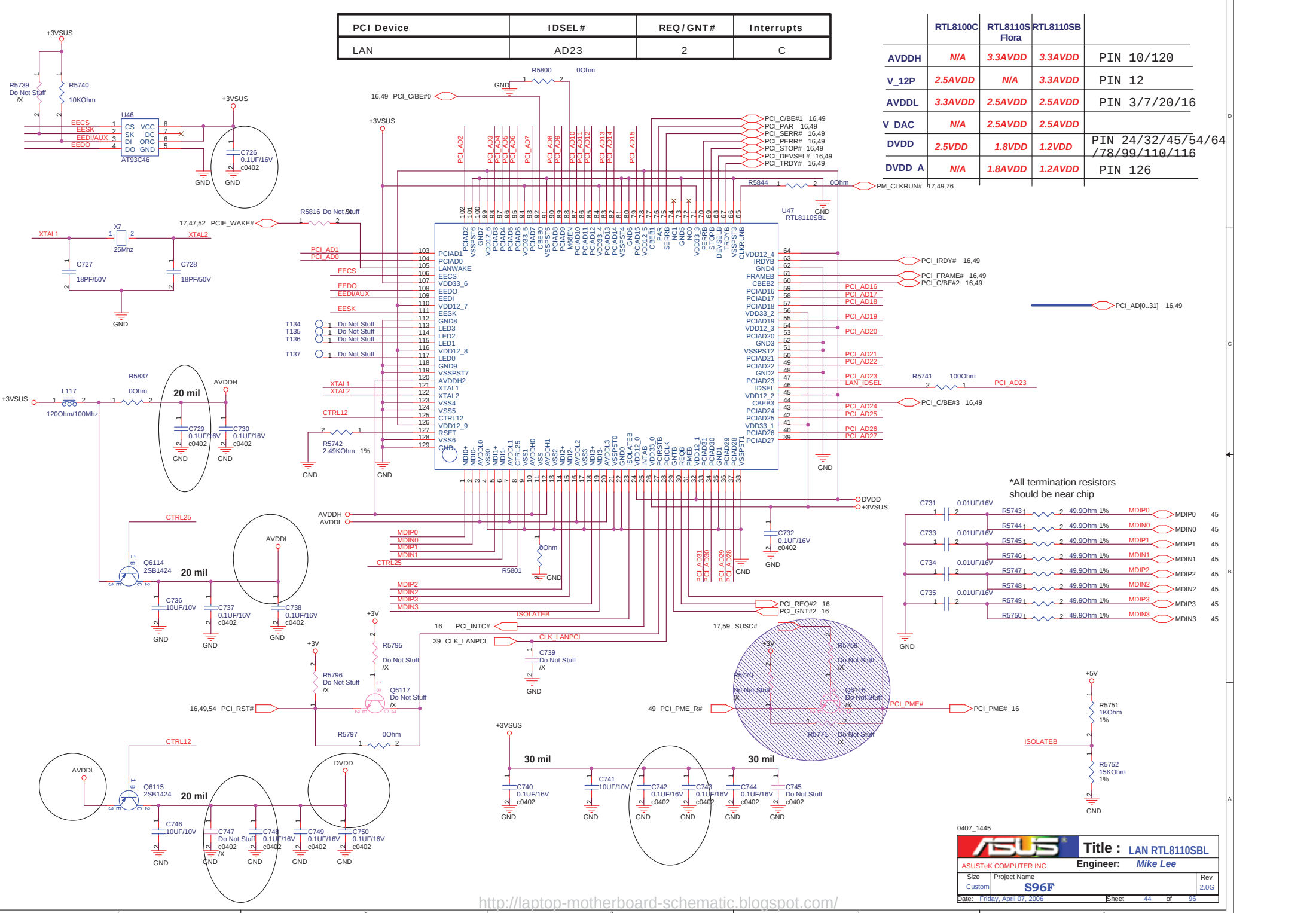


0407\_1445



0407\_1445

|                              |                             |                                        |          |
|------------------------------|-----------------------------|----------------------------------------|----------|
| <b>ASUS</b>                  |                             | <b>Title : DISCHARGE &amp; EMI CAP</b> |          |
| ASUSTeK COMPUTER INC. NB1    |                             | Engineer: <b>Mike Lee</b>              |          |
| Size<br>Custom               | Project Name<br><b>S96F</b> | Rev<br>2.0G                            |          |
| Date: Friday, April 07, 2006 |                             | Sheet                                  | 42 of 96 |



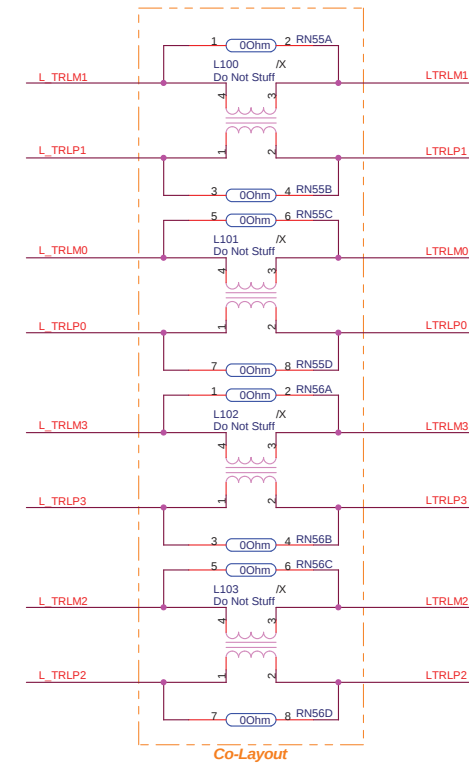
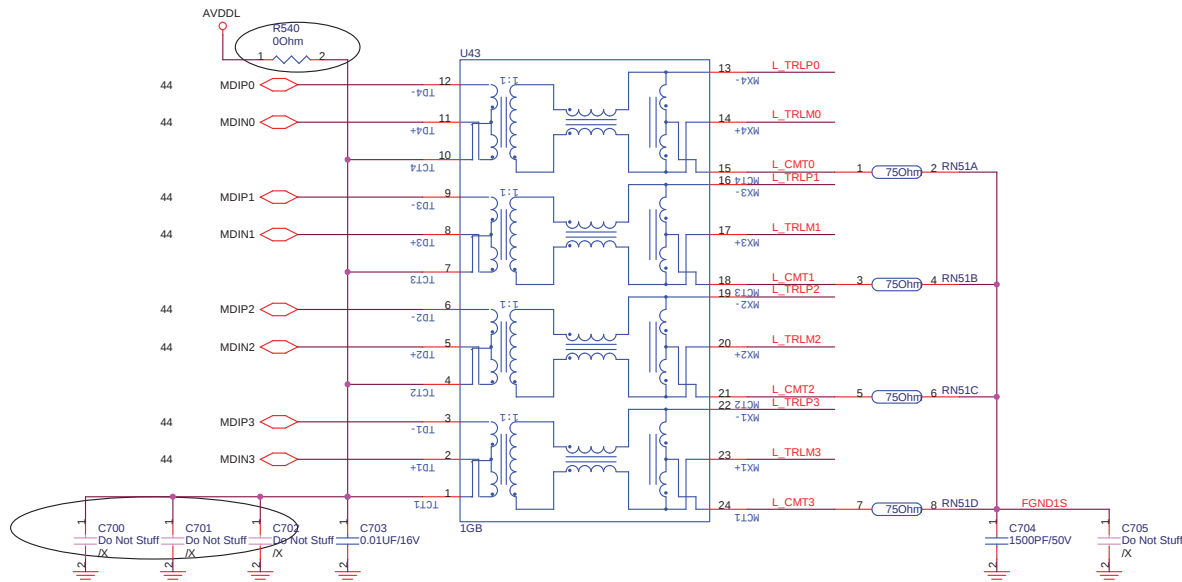
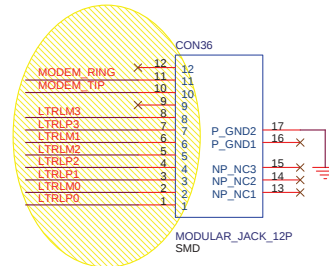
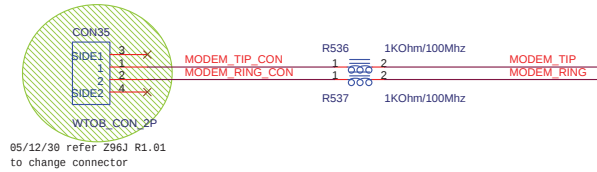
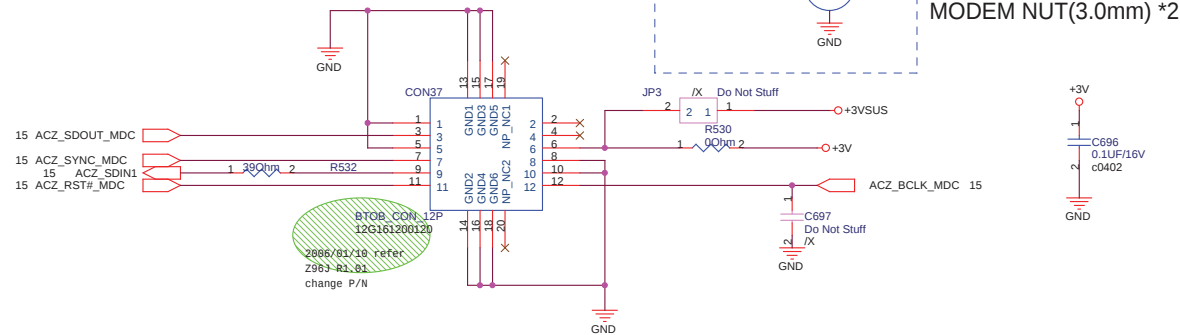
| PCI Device | IDSEL# | REQ / GNT# | Interrupts |
|------------|--------|------------|------------|
| LAN        | AD23   | 2          | C          |

|        | RTL8100C | RTL8110S<br>Flora | RTL8110SB |                                      |
|--------|----------|-------------------|-----------|--------------------------------------|
| AVDDH  | N/A      | 3.3AVDD           | 3.3AVDD   | PIN 10/120                           |
| V_12P  | 2.5AVDD  | N/A               | 3.3AVDD   | PIN 12                               |
| AVDDL  | 3.3AVDD  | 2.5AVDD           | 2.5AVDD   | PIN 3/7/20/16                        |
| V_DAC  | N/A      | 2.5AVDD           | 2.5AVDD   | PIN 24/32/45/54/64<br>/78/99/110/116 |
| DVDD   | 2.5VDD   | 1.8VDD            | 1.2VDD    | PIN 126                              |
| DVDD_A | N/A      | 1.8AVDD           | 1.2AVDD   |                                      |

0407\_1445

|                              |                             |                        |  |
|------------------------------|-----------------------------|------------------------|--|
| <b>ASUS</b>                  |                             | Title : LAN RTL8110SBL |  |
| ASUSTeK COMPUTER INC         |                             | Engineer: Mike Lee     |  |
| Size<br>Custom               | Project Name<br><b>S96F</b> | Rev<br>2.0G            |  |
| Date: Friday, April 07, 2006 |                             | Sheet 44 of 96         |  |

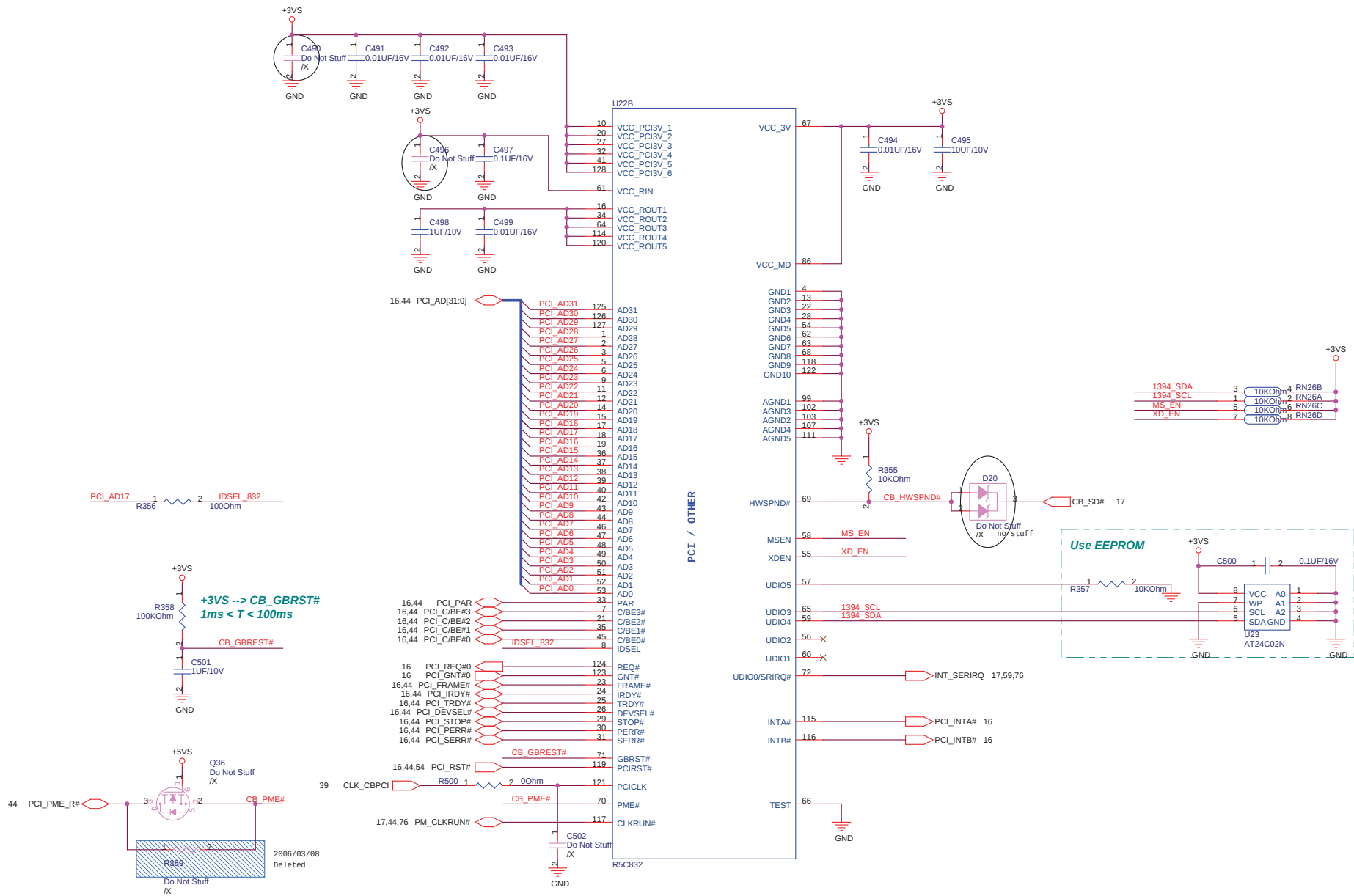
# MDC CONN.



0407\_1445

|                              |              |                              |       |
|------------------------------|--------------|------------------------------|-------|
| <b>ASUS</b>                  |              | Title : <b>RJ45&amp;RJ11</b> |       |
| ASUSTeK COMPUTER INC.        |              | Engineer: <b>Mike Lee</b>    |       |
| Size                         | Project Name | Rev                          |       |
| Custom                       | <b>S96F</b>  | 2.0G                         |       |
| Date: Friday, April 07, 2006 | Sheet        | 45                           | of 96 |





| PCI Device  | IDSEL# | REQ / GNT# | Interrupts |
|-------------|--------|------------|------------|
| CARD READER | AD17   | 0          | B          |
| 1394        | AD17   | 0          | A          |

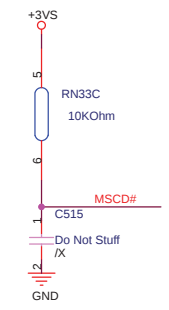
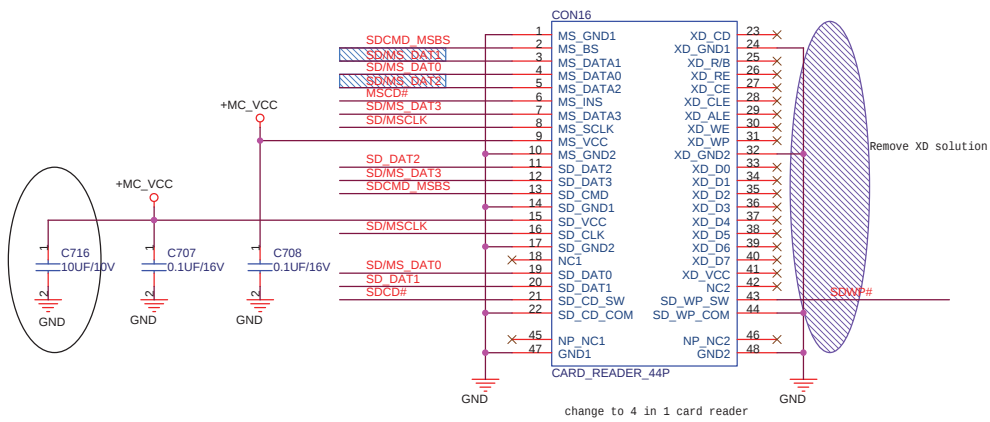
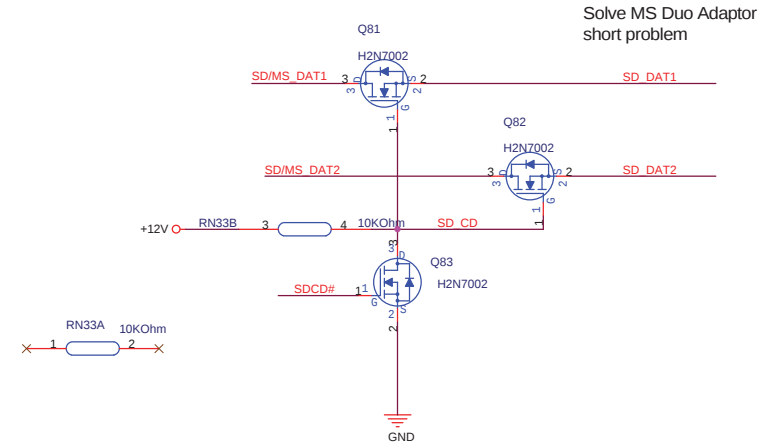
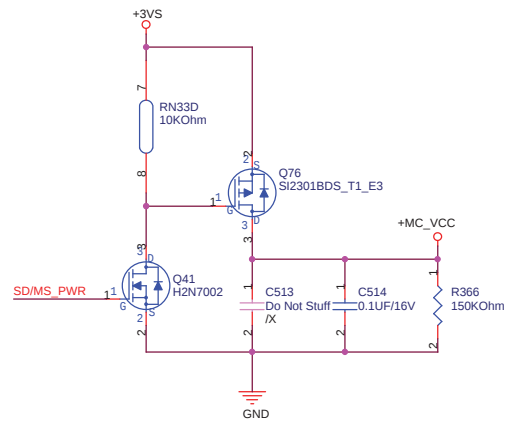
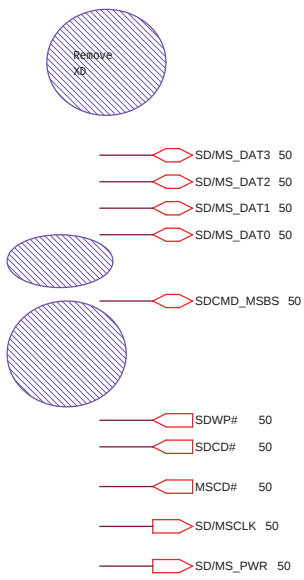
0407\_1445

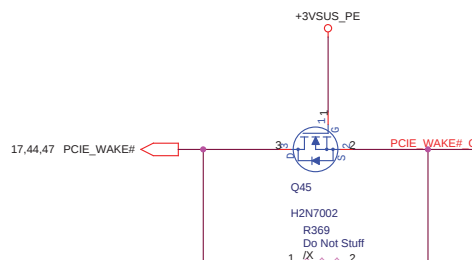
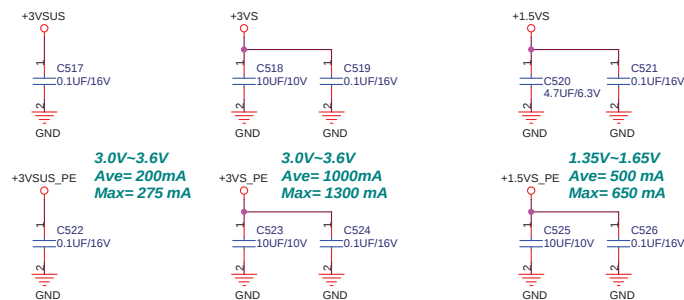
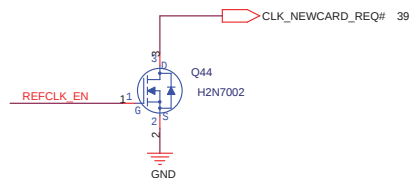
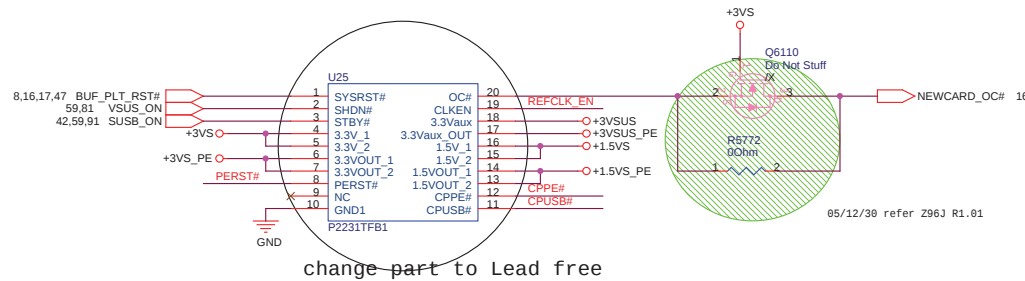
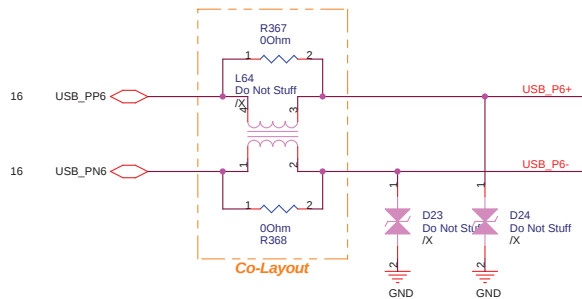
ASUS  
ASUSTek COMPUTER INC. MB6  
Size Custom  
Date: Friday, April 07, 2006

Title :CARD1394-R5C832(1)  
Engineer: Mike Lee  
Project Name  
S96F  
Rev 2.0G

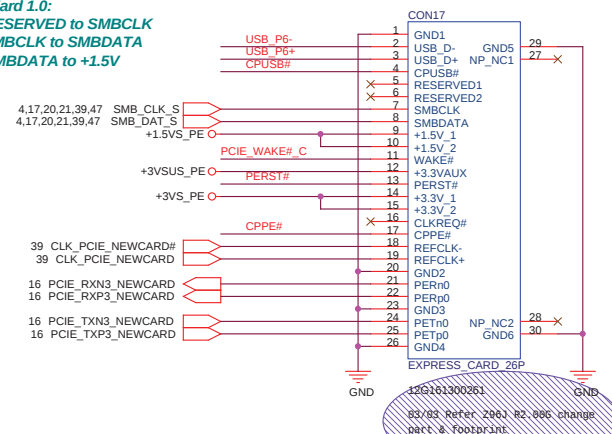
Sheet 49 of 96



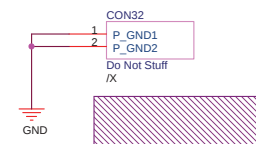




**!! ExpressCard Standard 1.0:**  
 Change Pin7 from RESERVED to SMBCLK  
 Change Pin8 from SMBCLK to SMBDATA  
 Change Pin9 from SMBDATA to +1.5V

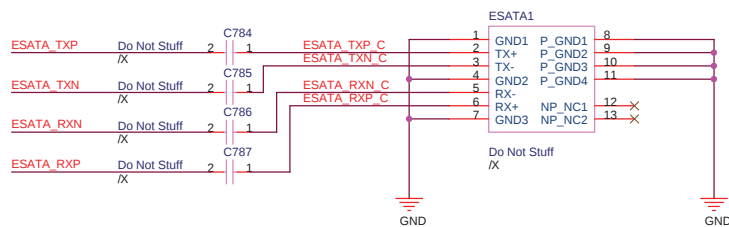
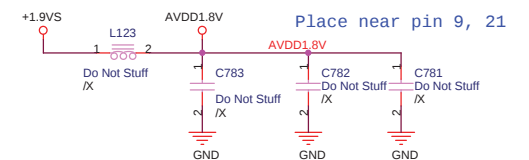
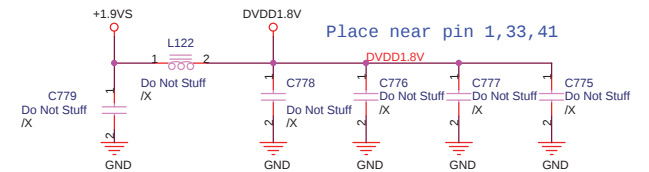
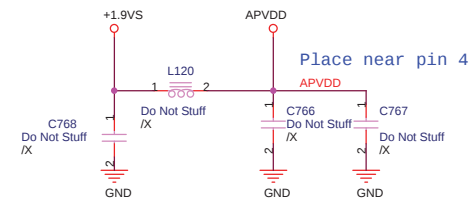
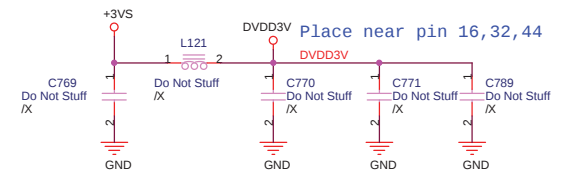
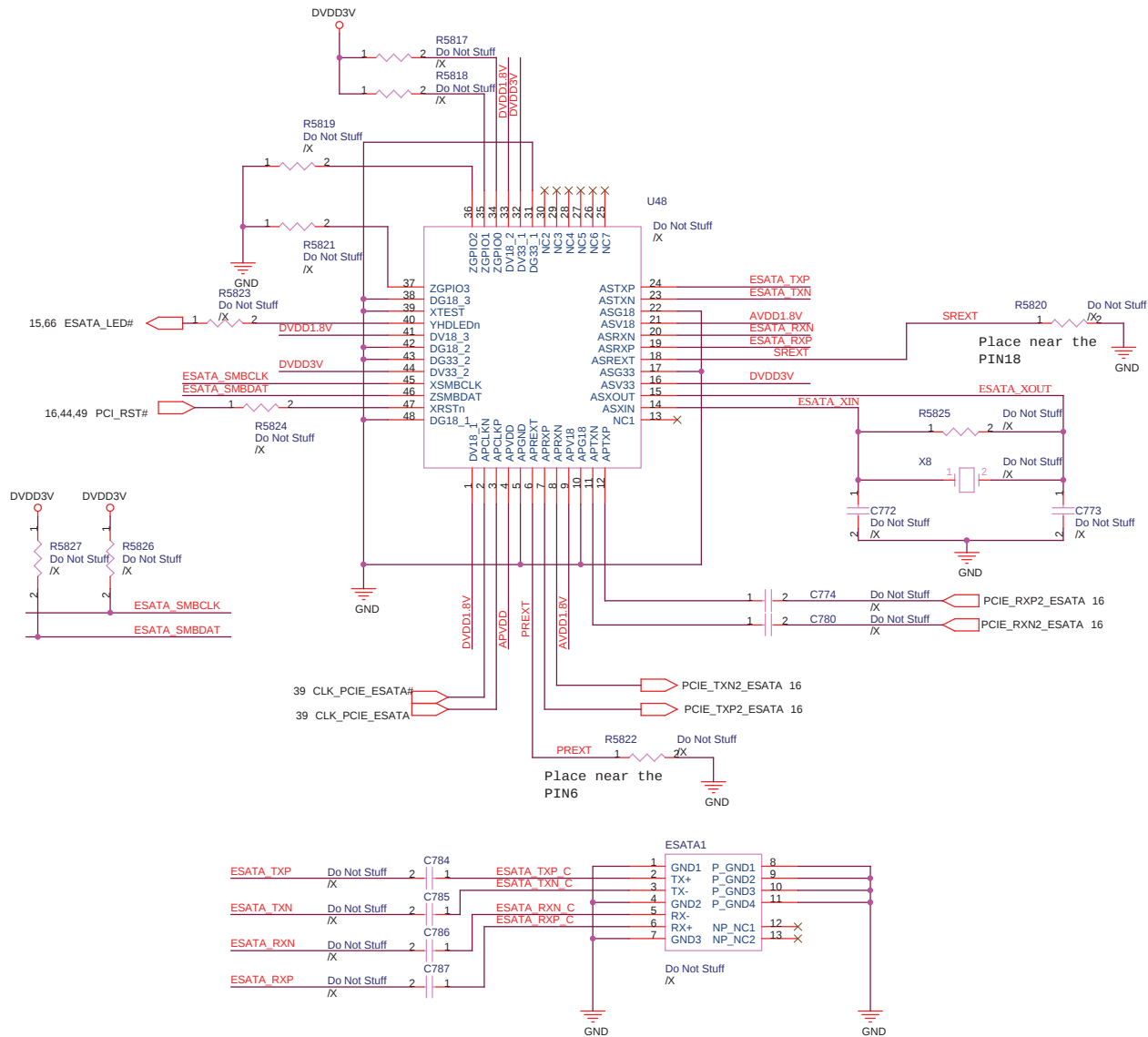


**NewCard Ejecter**



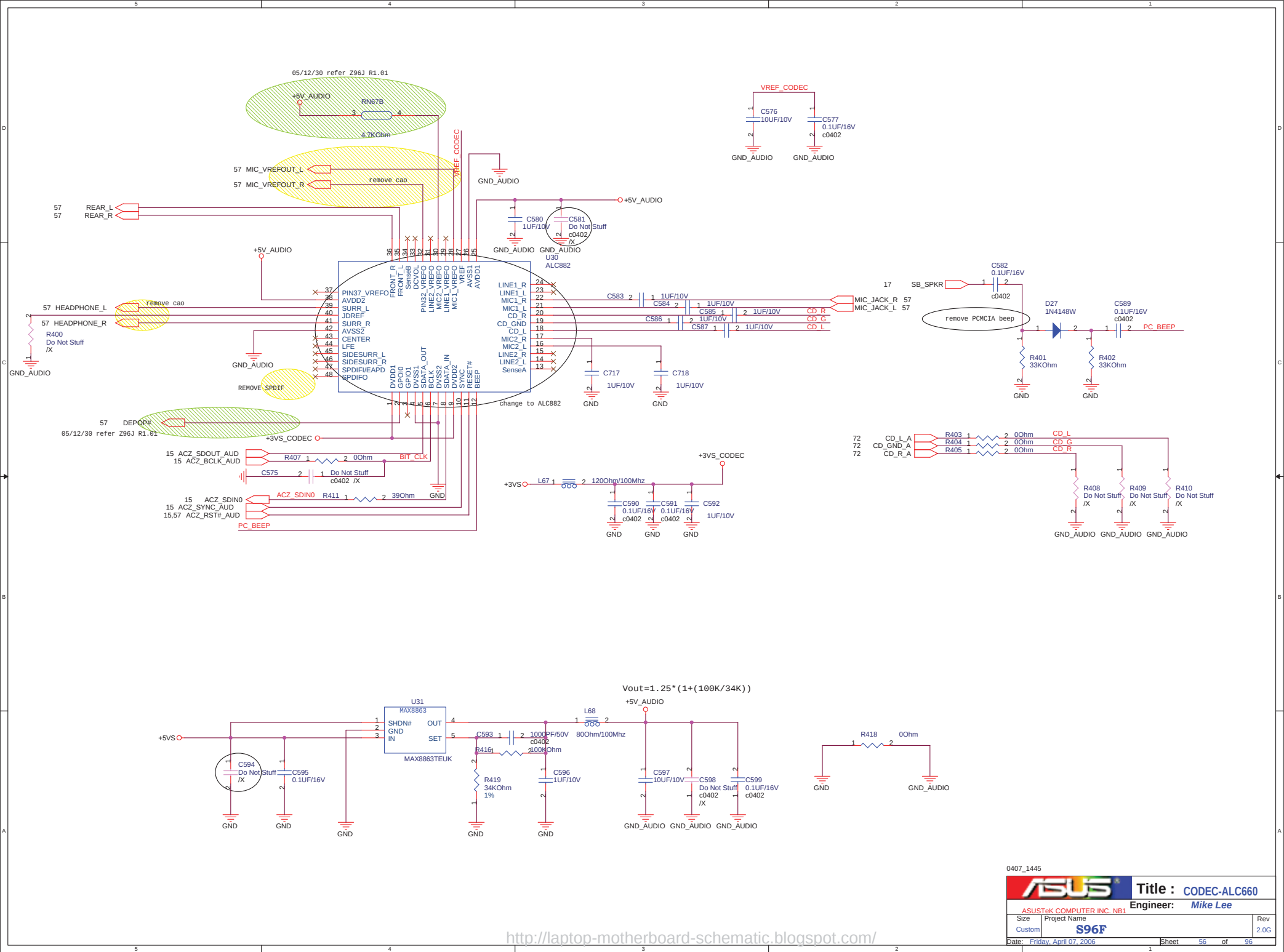
0407\_1445

|                              |              |                           |       |
|------------------------------|--------------|---------------------------|-------|
| <b>ASUS</b>                  |              | Title : <b>NEWCARD</b>    |       |
| ASUSTek COMPUTER INC. NB1    |              | Engineer: <b>Mike Lee</b> |       |
| Size                         | Project Name | Rev                       |       |
| Custom                       | <b>S96F</b>  | 2.0G                      |       |
| Date: Friday, April 07, 2006 | Sheet        | 52                        | of 96 |

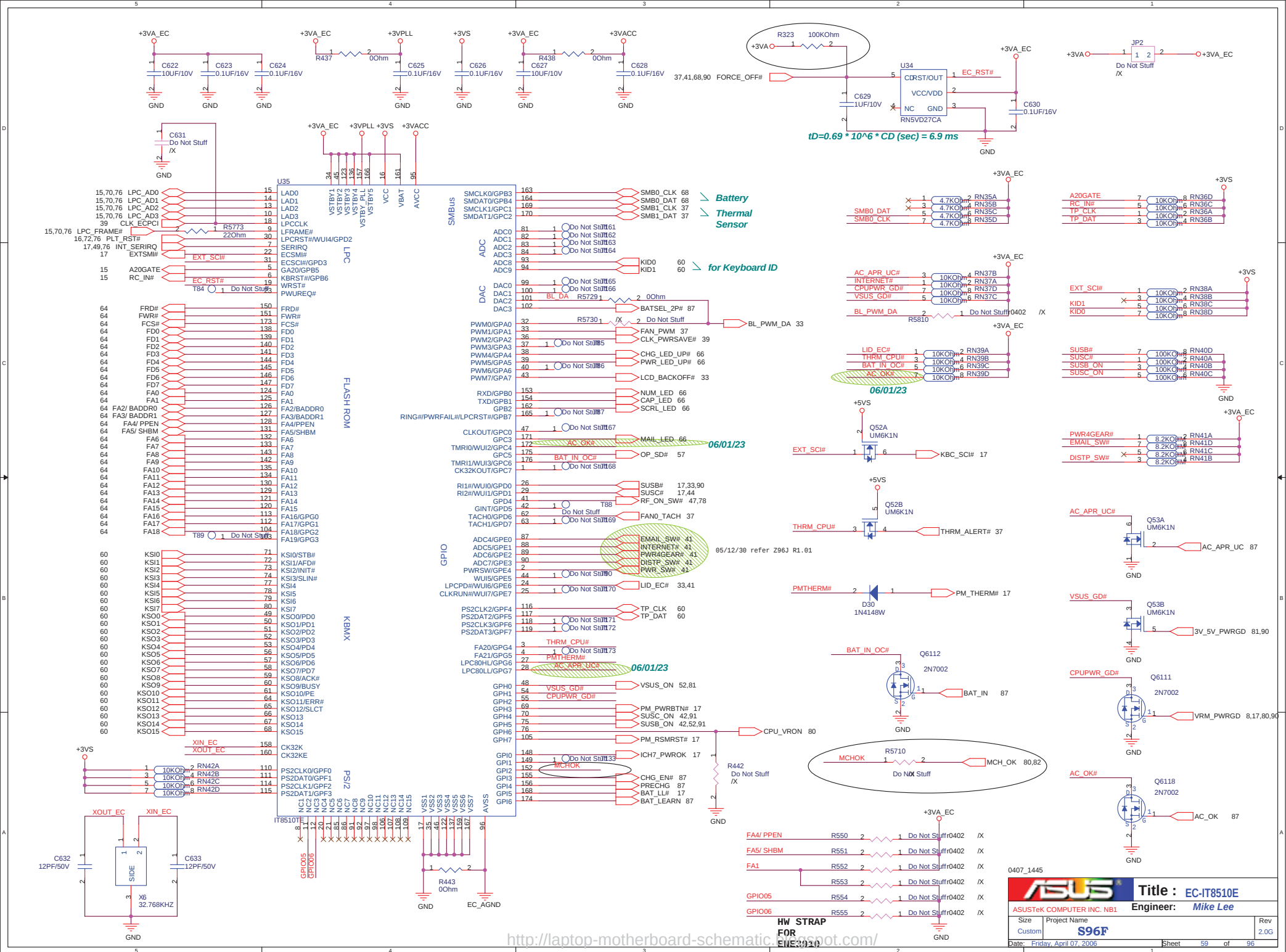


0407\_1445

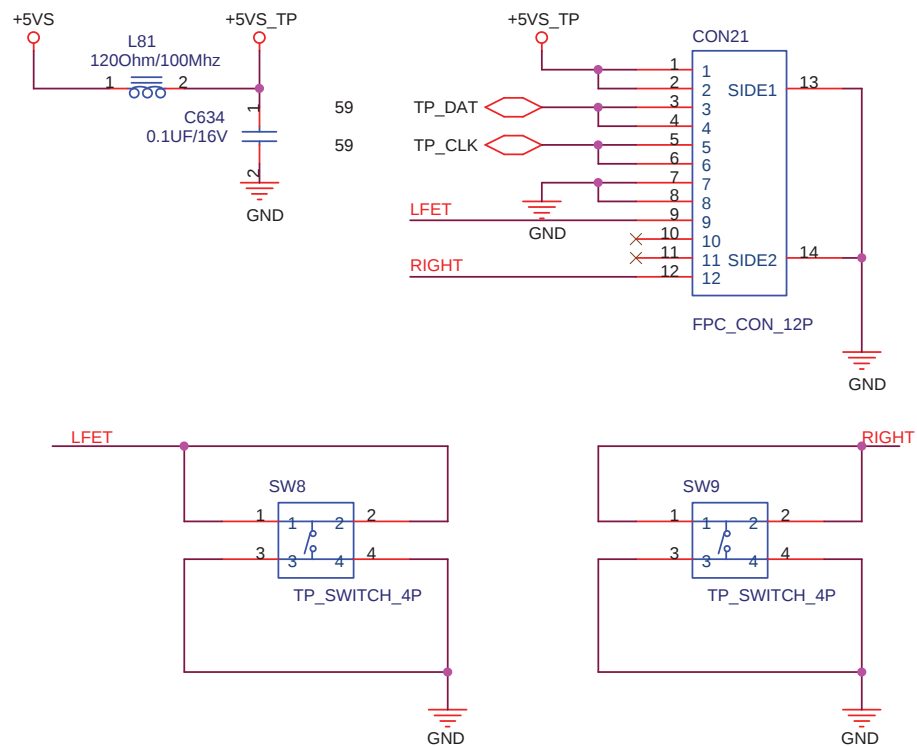
|                              |              |                    |       |
|------------------------------|--------------|--------------------|-------|
| <b>ASUS</b>                  |              | Title : ESATA      |       |
| ASUSTek COMPUTER INC         |              | Engineer: Mike Lee |       |
| Size                         | Project Name | Rev                |       |
| A3                           | S96F         | 2.0G               |       |
| Date: Friday, April 07, 2006 | Sheet        | 54                 | of 96 |



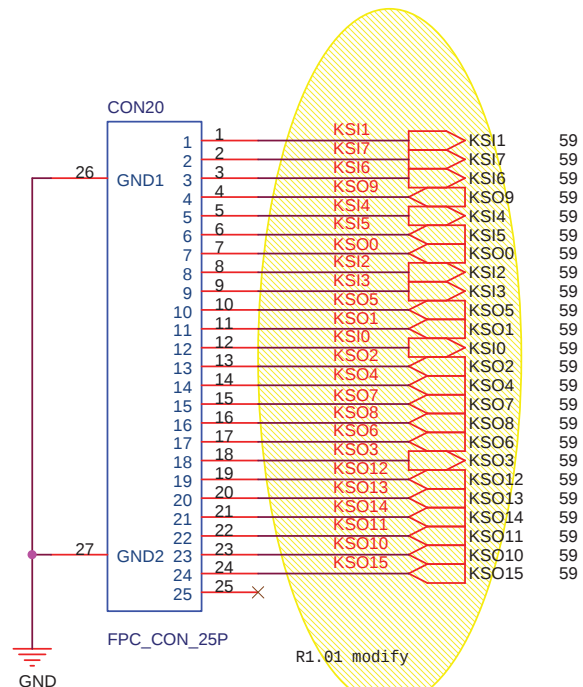




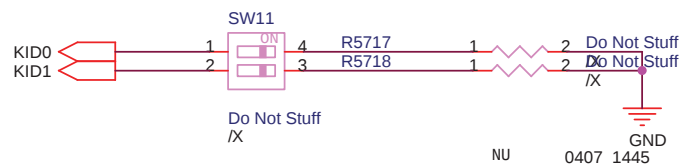
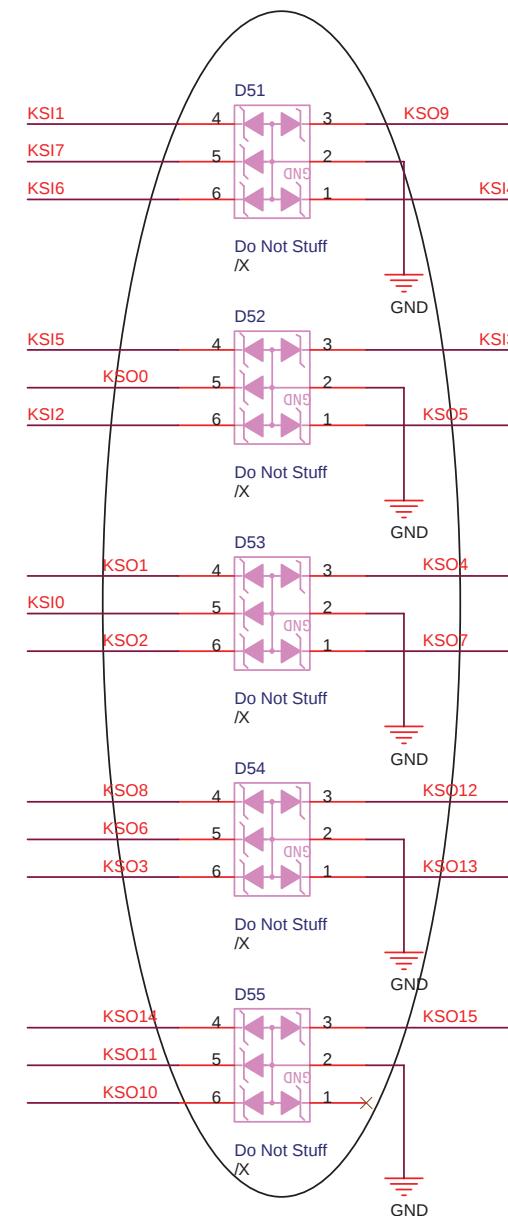
### *For Touch-Pad*

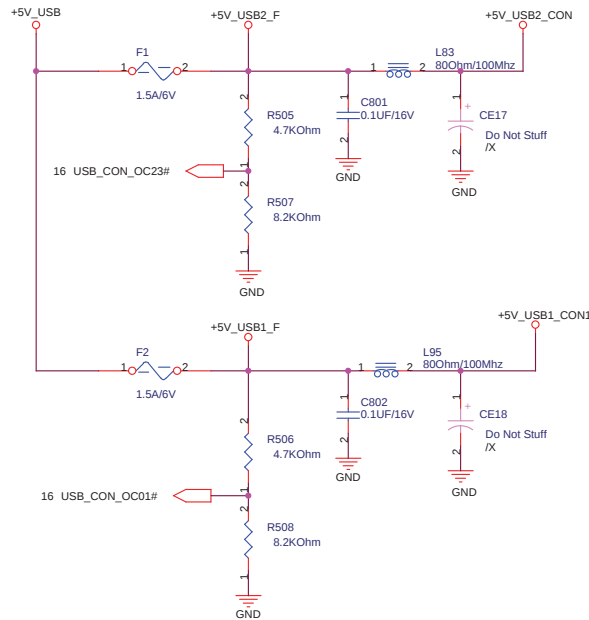
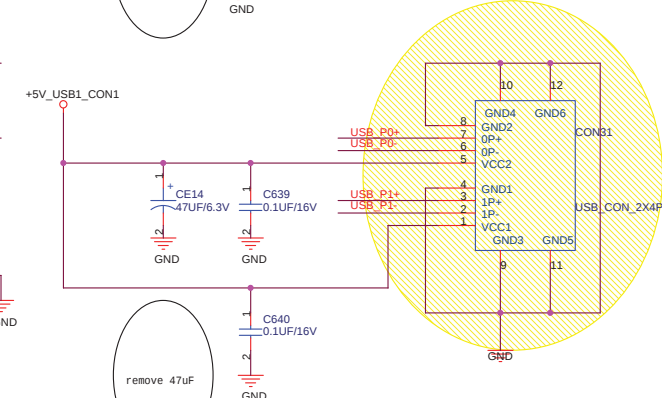
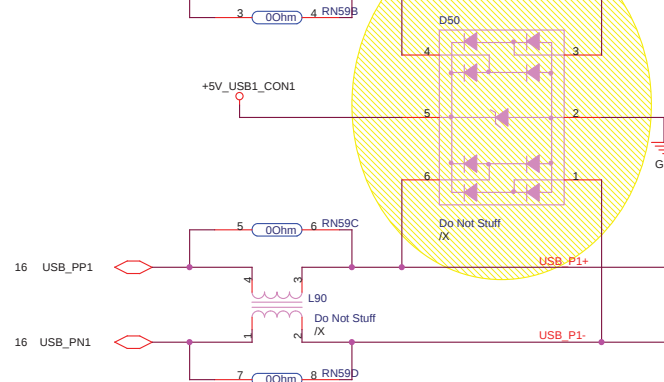
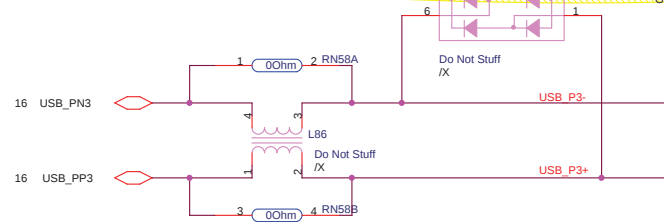
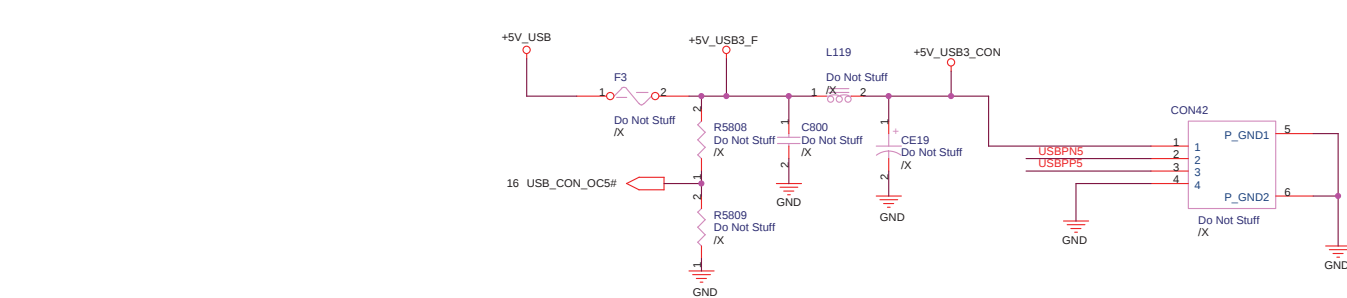


### *For Keyboard*



05/12/29 ESD DIODE PIN SWAPPED



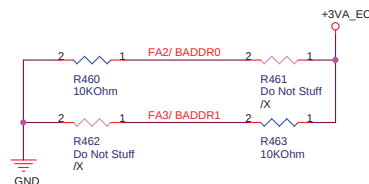


# ISA ROM

## EC Hardware Strapping

### FA2/ BADDR0 & FA3/ BADDR1

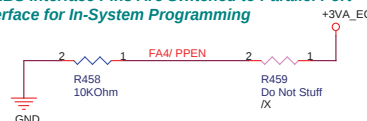
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

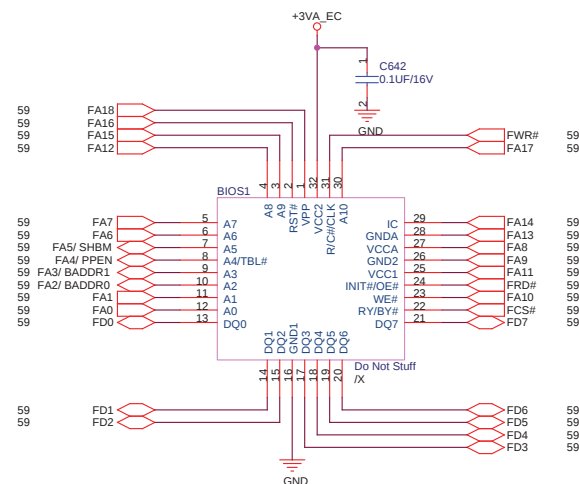
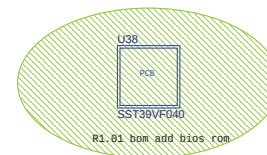
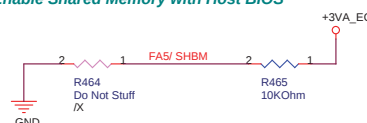
### FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



### FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

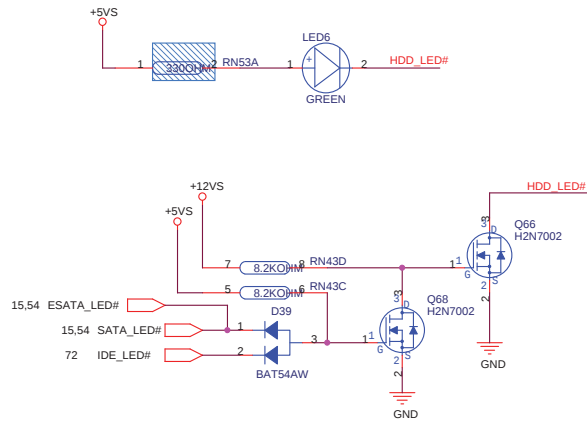


0407\_1445

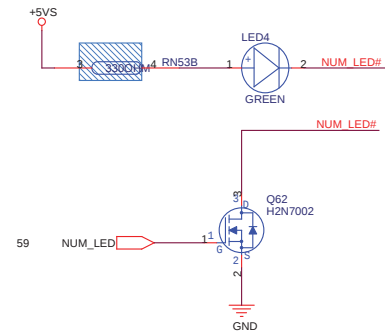
|                              |              |                    |  |
|------------------------------|--------------|--------------------|--|
| <b>ASUS</b>                  |              | Title :ISA ROM     |  |
| ASUSTek COMPUTER INC. NB1    |              | Engineer: Mike Lee |  |
| Size                         | Project Name | Rev                |  |
| Custom                       | S96F         | 2.0G               |  |
| Date: Friday, April 07, 2006 |              | Sheet 64 of 96     |  |

# For LED

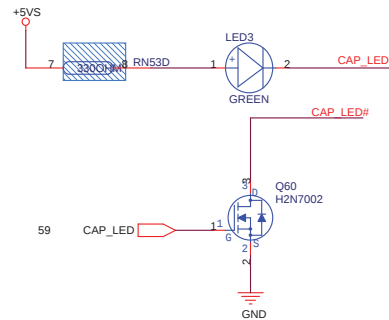
## For SATA/IDE LED



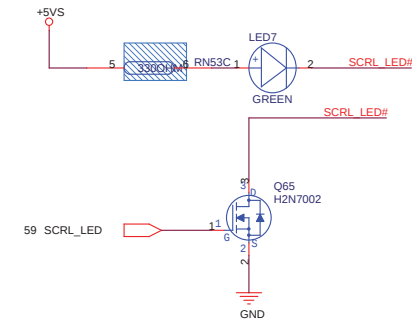
## for Num Lock



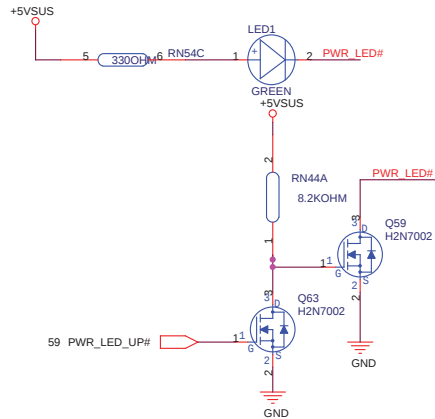
## for Cap. Lock



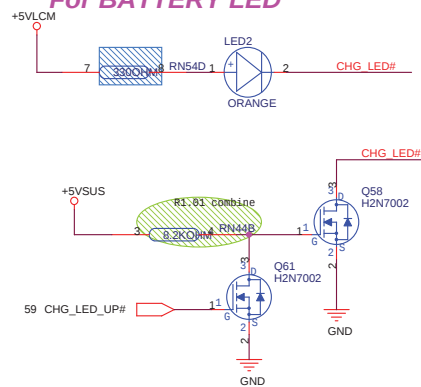
## for Scroll Lock



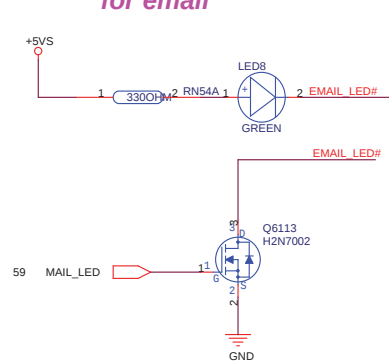
## For POWER LED



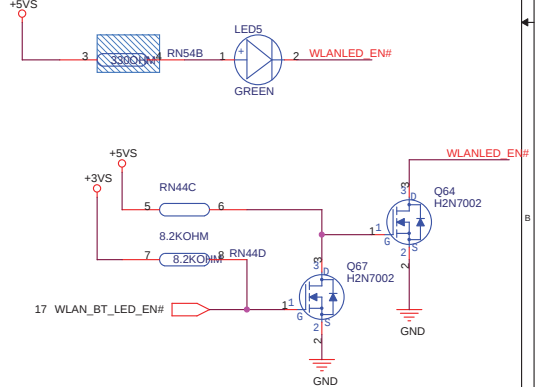
## For BATTERY LED



## for email



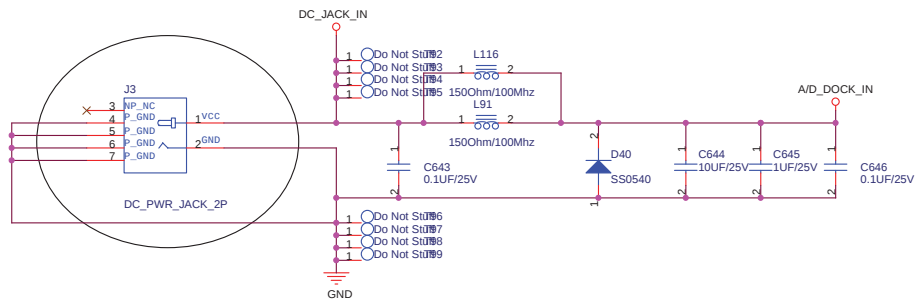
## For WireLess LED



0407\_1445

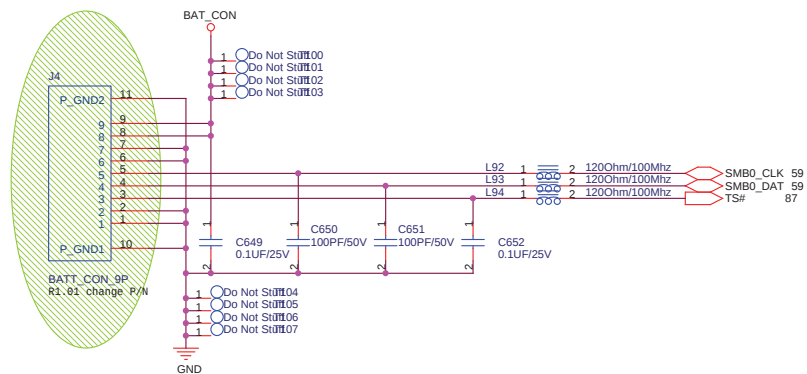
|                              |              |                    |          |
|------------------------------|--------------|--------------------|----------|
| <b>ASUS</b>                  |              | Title : LED        |          |
| ASUSTeK COMPUTER INC         |              | Engineer: Mike Lee |          |
| Size                         | Project Name | Rev                |          |
| Custom                       | S96F         | 2.0G               |          |
| Date: Friday, April 07, 2006 |              | Sheet              | 66 of 96 |

## DC IN

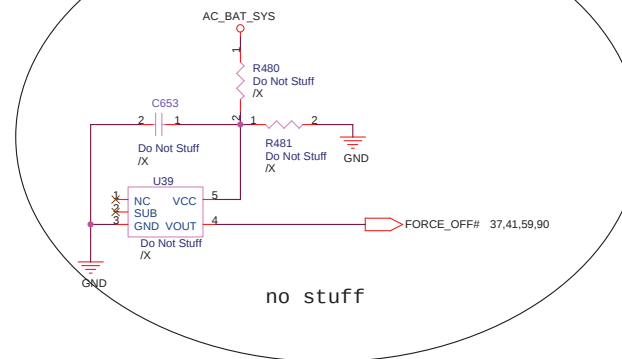


remove AC DC detect; no need

## BAT IN



## Without Battery & Pull out Adapter

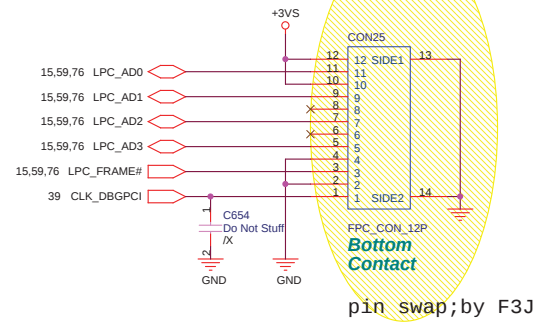


no stuff

0407\_1445

|                              |              |                     |          |
|------------------------------|--------------|---------------------|----------|
| <b>ASUS</b>                  |              | Title : DC & BAT IN |          |
| ASUSTek COMPUTER INC. NBI    |              | Engineer: Mike Lee  |          |
| Size                         | Project Name | Rev                 |          |
| Custom                       | S96F         | 2.0G                |          |
| Date: Friday, April 07, 2006 |              | Sheet               | 68 of 96 |

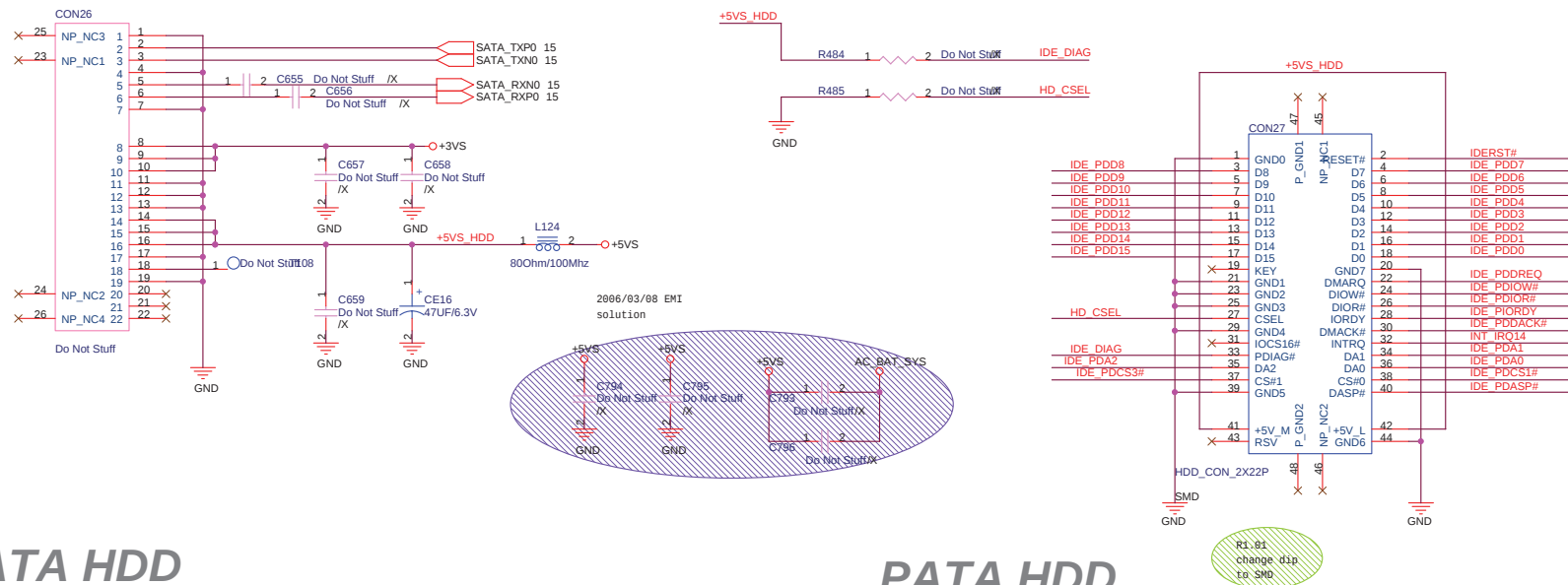
*For Debug*



0407\_1445

|                              |              |                            |       |
|------------------------------|--------------|----------------------------|-------|
| <b>ASUS</b>                  |              | <b>Title : Debug CONN.</b> |       |
| ASUSTeK COMPUTER INC         |              | Engineer: <i>Mike Lee</i>  |       |
| Size                         | Project Name | Rev                        |       |
| Custom                       | <b>S96F</b>  | 2.0G                       |       |
| Date: Friday, April 07, 2006 | Sheet        | 70                         | of 96 |

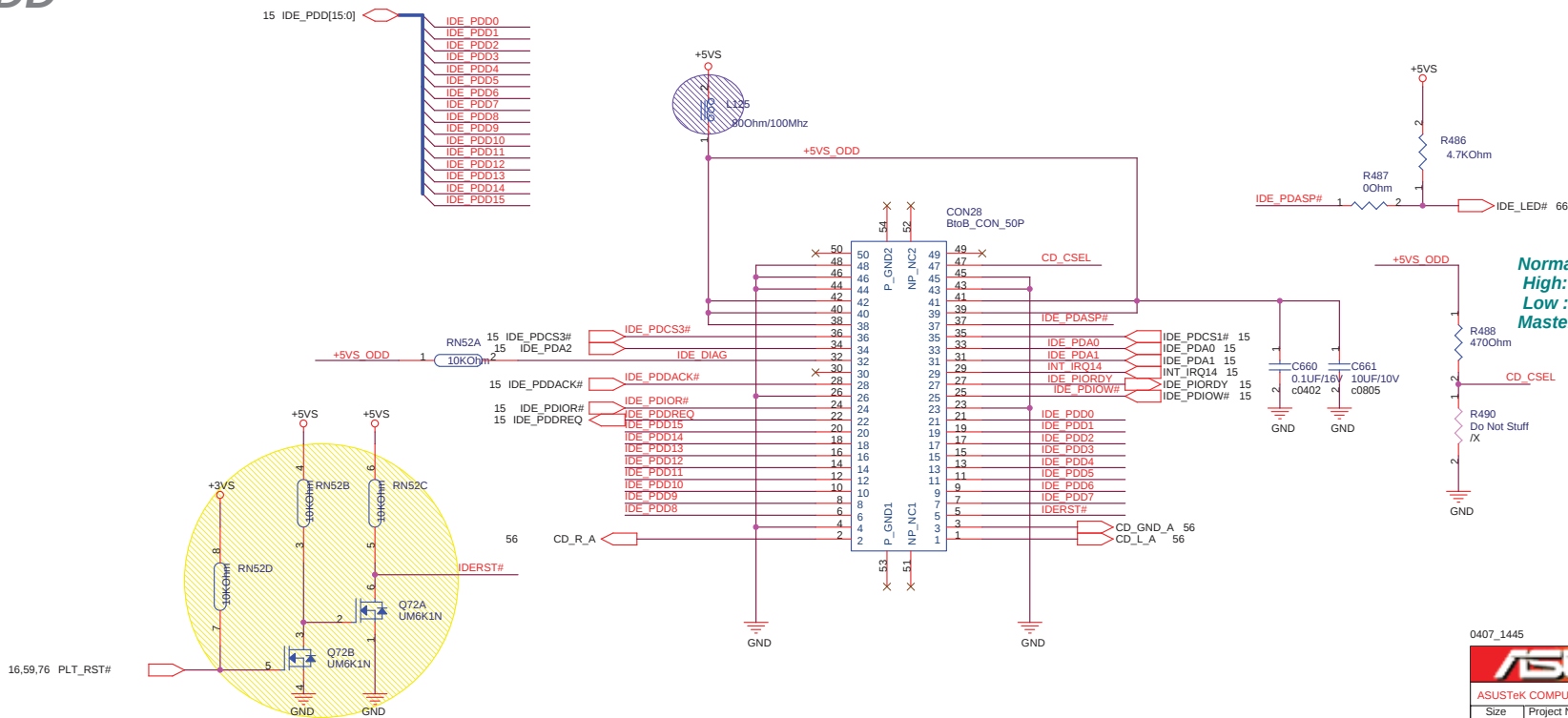
HD\_CSEL : Pull-Down, HDD as Master



## SATA HDD

## PATA HDD

**ODD**



Normal type  
High: Slave  
Low :  
Master

0407\_1445



**Title :** SATA-HDD & ODD

ASUSTeK COMPUTER INC. NB1

Engineer: *Mike Lee*

| Size | Project Name |
|------|--------------|
|------|--------------|

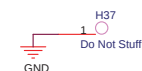
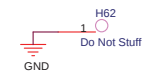
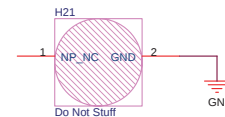
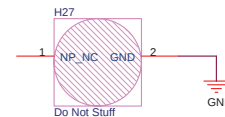
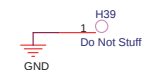
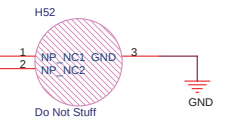
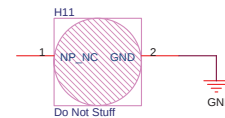
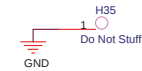
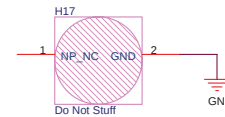
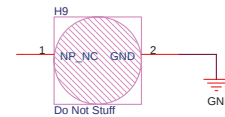
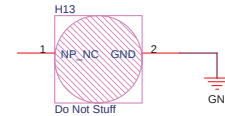
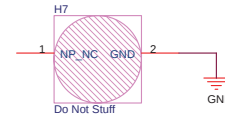
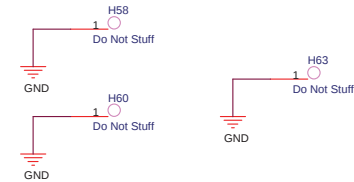
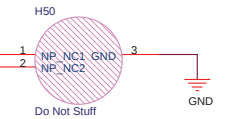
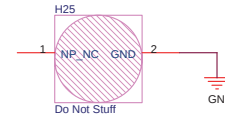
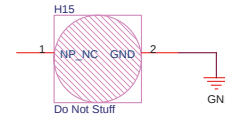
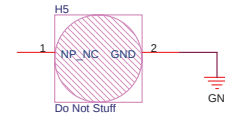
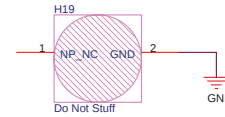
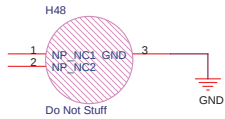
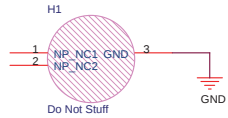
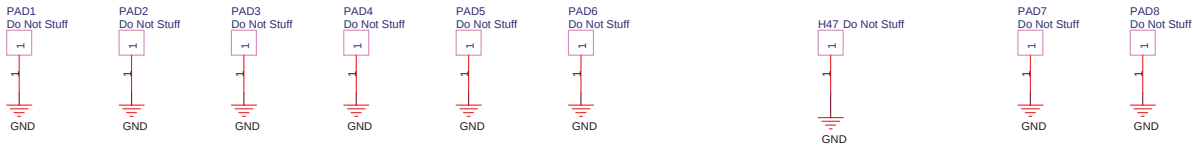
Student Name \_\_\_\_\_

|  |     |
|--|-----|
|  | Rev |
|--|-----|

Date: Friday, April 07, 2006

Sheet 72

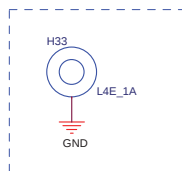
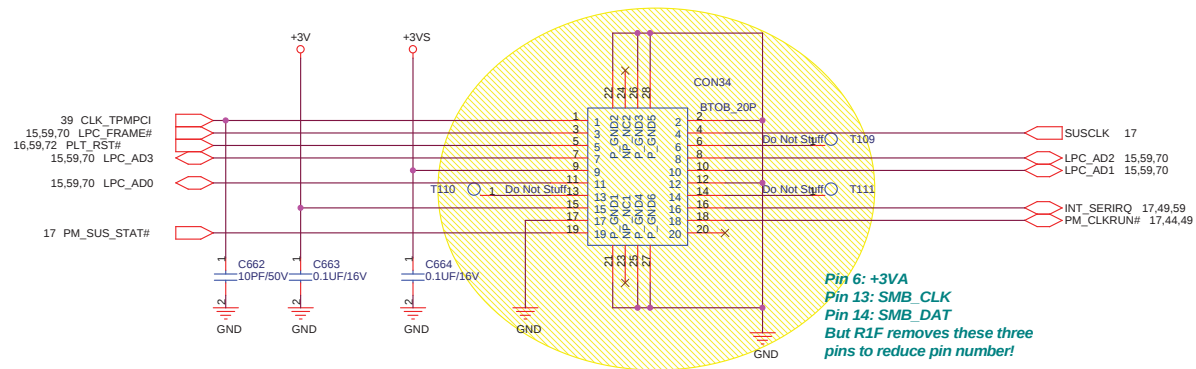
---



0407\_1445

|                              |              |                           |       |
|------------------------------|--------------|---------------------------|-------|
| <b>ASUS</b>                  |              | <b>Title : SCREW HOLE</b> |       |
| ASUSTek COMPUTER INC         |              | Engineer: <b>Mike Lee</b> |       |
| Size                         | Project Name | Rev                       |       |
| Custom                       | <b>S96F</b>  | 2.0G                      |       |
| Date: Friday, April 07, 2006 | Sheet        | 74                        | of 96 |

## For TPM Module

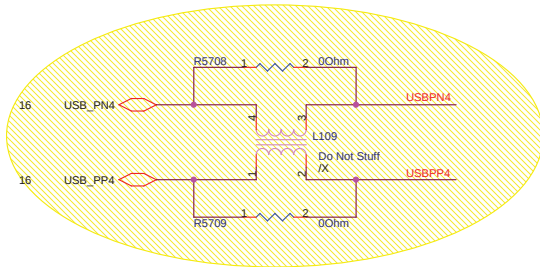
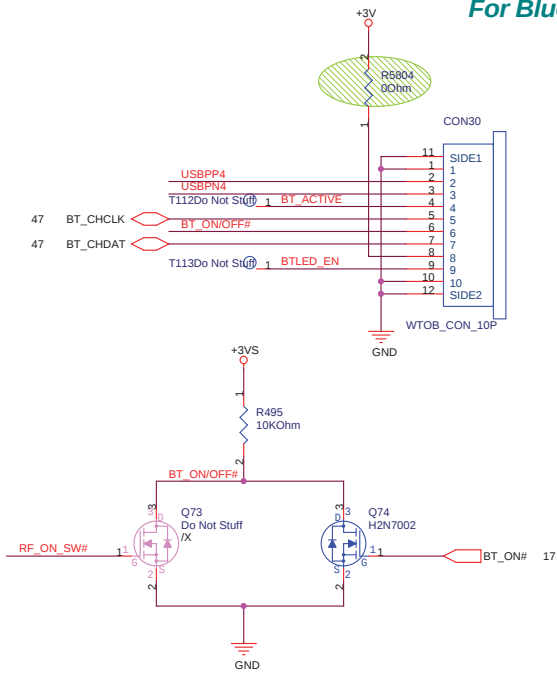


TPM MODULE NUT(3.0mm) \*1

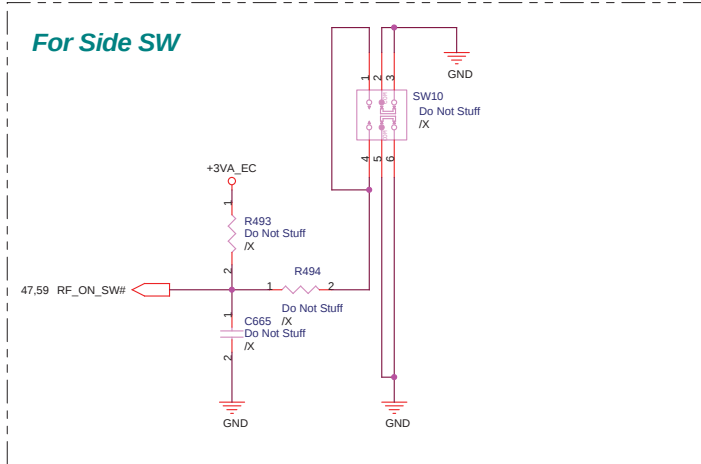
0407\_1445

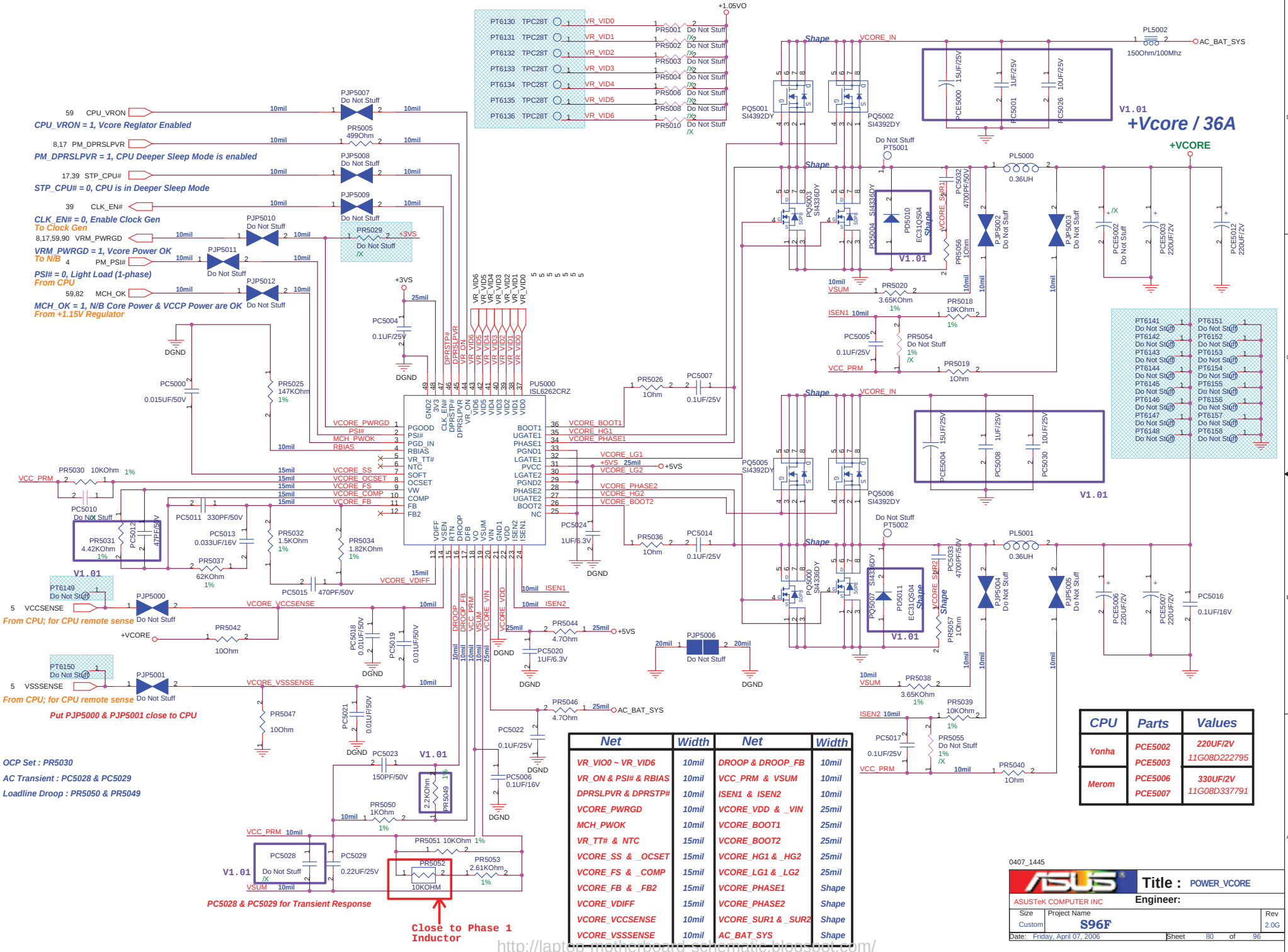
|                              |              |                    |          |
|------------------------------|--------------|--------------------|----------|
| <b>ASUS</b>                  |              | Title : TPM        |          |
| ASUSTek COMPUTER INC         |              | Engineer: Mike Lee |          |
| Size                         | Project Name | Rev                |          |
| Custom                       | S96F         | 2.0G               |          |
| Date: Friday, April 07, 2006 |              | Sheet              | 76 of 96 |

### For Bluetooth



***For Side SW***





| Net                  | Width | Net                | Width |
|----------------------|-------|--------------------|-------|
| VR_VIO0 ~ VR_VIO6    | 10mil | DROOP & DROOP_FB   | 10mil |
| VR_ON & PSI# & RBIAS | 10mil | VCC_PRM & VSUM     | 10mil |
| DPRSLPVR & DPRSTP#   | 10mil | ISEN1 & ISEN2      | 10mil |
| VCORE_PWRGD          | 10mil | VCORE_VDD & _VIN   | 25mil |
| MCH_PWOK             | 10mil | VCORE_BOOT1        | 25mil |
| VR_TT# & NTC         | 15mil | VCORE_BOOT2        | 25mil |
| VCORE_SS & OCSET     | 15mil | VCORE_HG1 & _HG2   | 25mil |
| VCORE_FS & COMP      | 15mil | VCORE_LG1 & _LG2   | 25mil |
| VCORE_FB & FB2       | 15mil | VCORE_PHASE1       | Shape |
| VCORE_VDIFF          | 15mil | VCORE_PHASE2       | Shape |
| VCORE_VCCSENSE       | 10mil | VCORE_SUR1 & _SUR2 | Shape |
| VCORE_VSSSENSE       | 10mil | AC BAT SYS         | Shape |

| CPU   | Parts   | Values       |
|-------|---------|--------------|
| Yonha | PCE5002 | 220UF/2V     |
|       | PCE5003 | 11G08D222795 |
| Merom | PCE5006 | 330UF/2V     |
|       | PCE5007 | 11G08D337791 |

0407\_1445

Title : POWER\_VCORE

ASUSTek COMPUTER INC Engineer:

|        |              |      |
|--------|--------------|------|
| Size   | Project Name | Rev  |
| Custom | S96F         | 2.0G |

|                              |                |
|------------------------------|----------------|
| Date: Friday, April 07, 2006 | Sheet 80 of 96 |
|------------------------------|----------------|



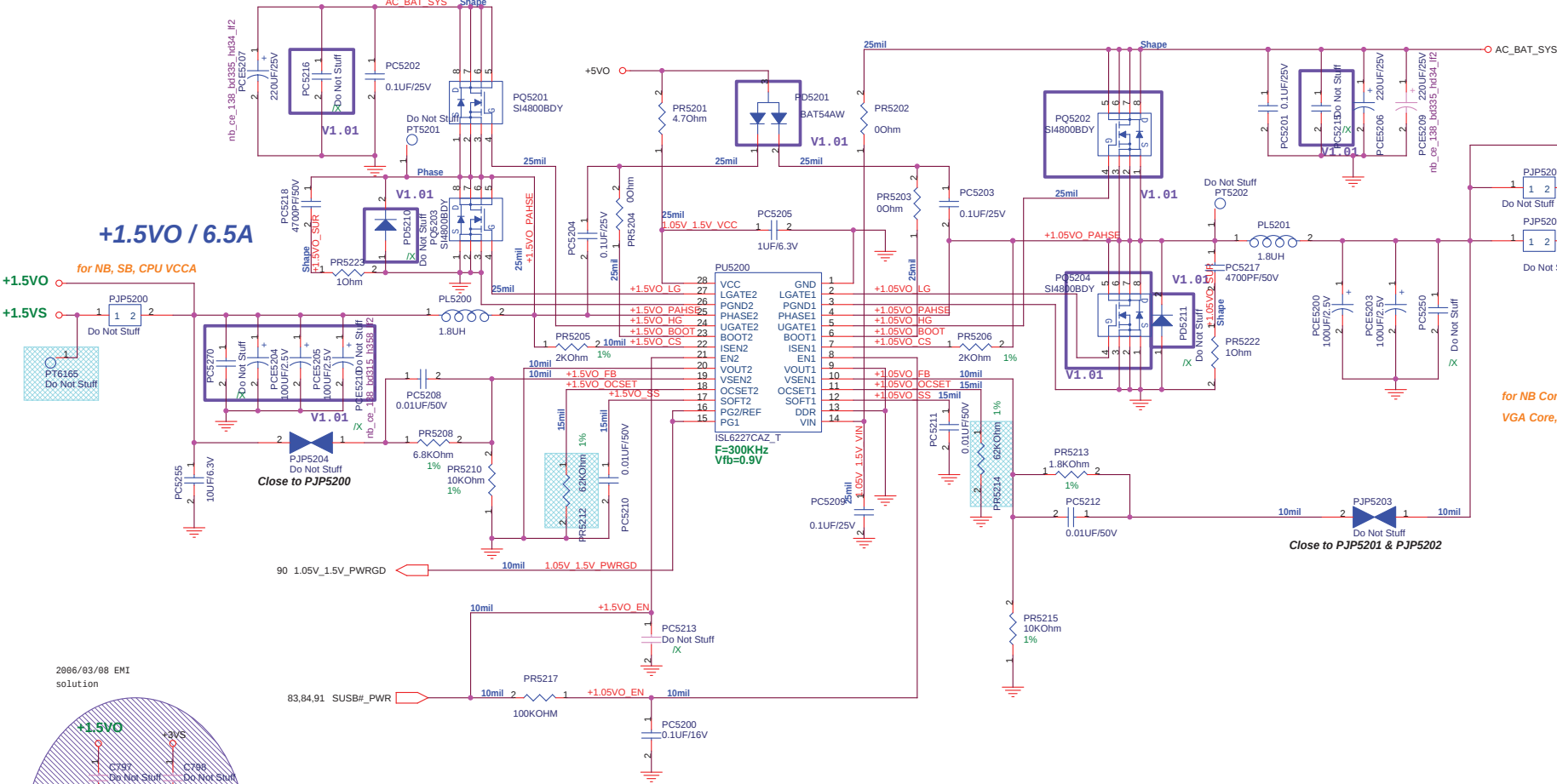
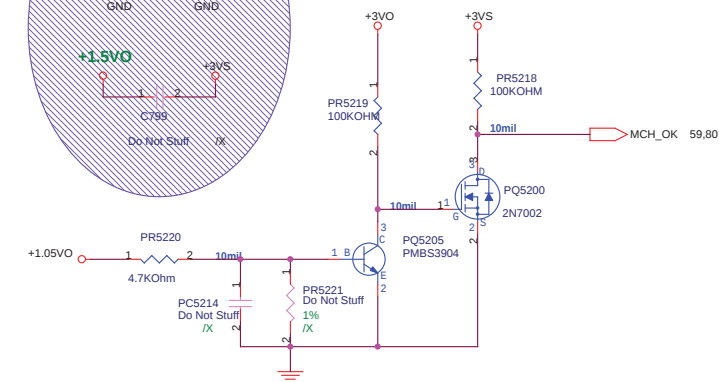
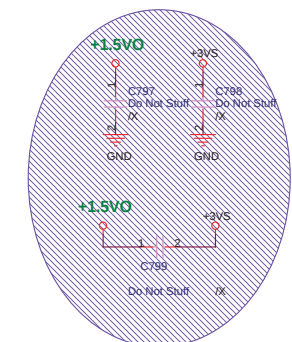
**+1.05VO / 10A**

**+1.5VO / 6.5A**

**+1.5VO for NB, SB, CPU VCCA**

**+1.5VS**

2006/03/08 EMI solution



**+1.05VO**  
**+VCCP**

for NB Core, SB Core, CPU VCCP  
VGA Core, VGA +1.2VSP

| Net              | Width | Net            | Width |
|------------------|-------|----------------|-------|
| 1.05V_1.5V_VCC   | 25mil | +1.5VO_SS      | 15mil |
| 1.05V_1.5V_PWRGD | 10mil | AC_BAT_SYS     | Shape |
| 1.05V_1.5V_VIN   | 25mil | +1.05VO_EN     | 10mil |
| +1.5VO_EN        | 10mil | +1.05VO_LG     | 25mil |
| +1.5VO_LG        | 25mil | +1.05VO_HG     | 25mil |
| +1.5VO_HG        | 25mil | +1.05VO_PHASE  | Shape |
| +1.5VO_PHASE     | Shape | +1.05VO_BOOT   | 25mil |
| +1.5VO_BOOT      | 25mil | +1.05VO_MODSEL | 10mil |
| +1.5VO_MODSEL    | 10mil | +1.05VO_CS     | 10mil |
| +1.5VO_CS        | 10mil | +1.05VO_FB     | 10mil |
| +1.5VO_FB        | 10mil | +1.05VO_OCSET  | 25mil |
| +1.5VO_OCSET     | 15mil | +1.05VO_SS     | 15mil |
| +1.5VO_SUR       | Shape | +1.05VO_SUR    | Shape |

0407\_1445

**Title :POWER\_I/O\_1.5VS & 1.05VS**

ASUSTek COMPUTER INC

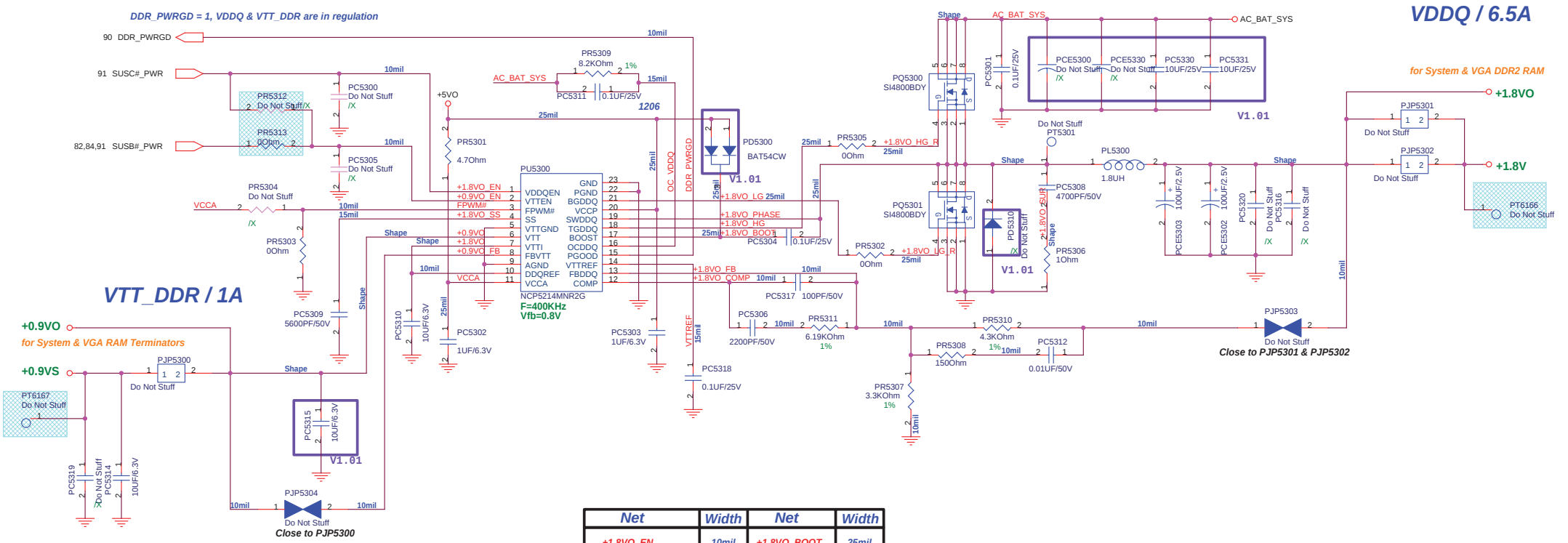
Engineer:

Size Project Name

Custom **S96F**

Rev 2.05

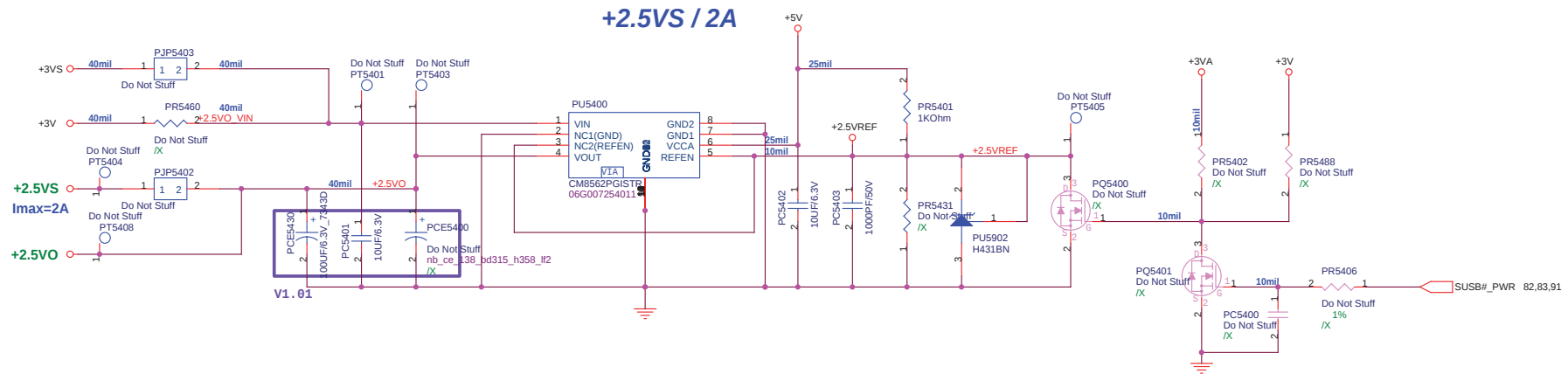
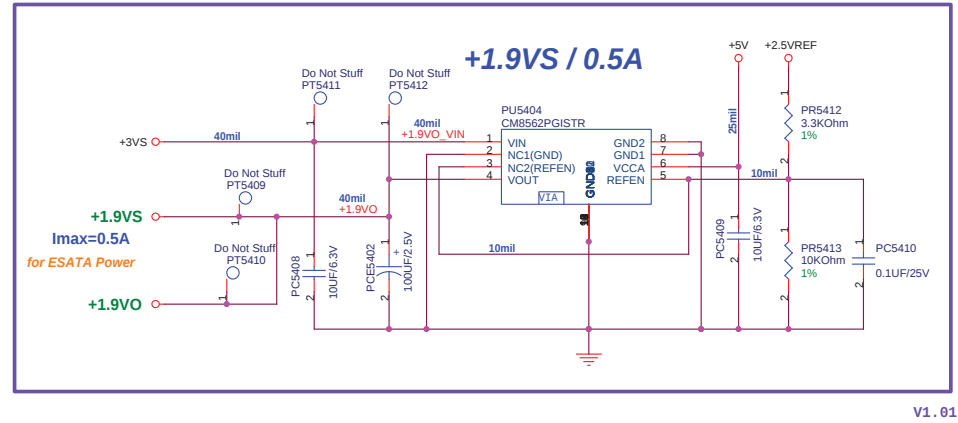
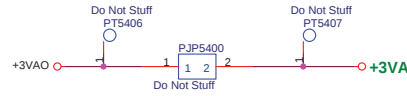
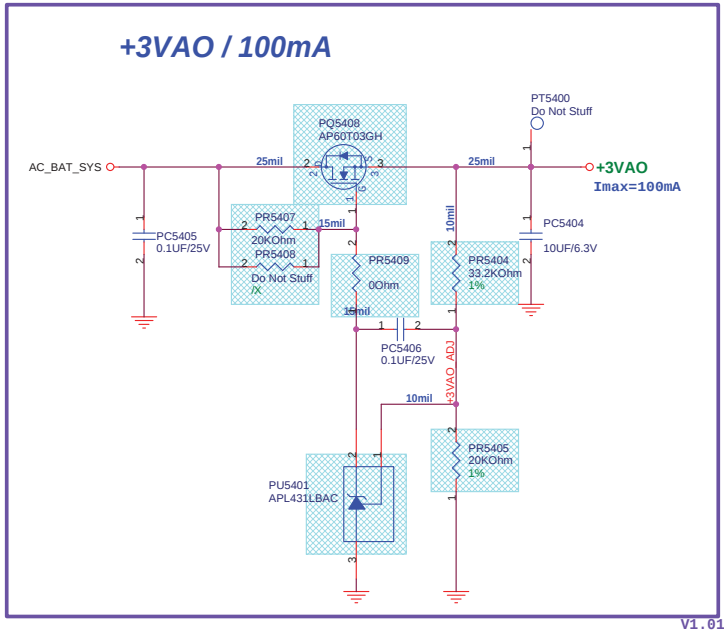
Date: Friday, April 07, 2006 Sheet 82 of 96



| Net               | Width | Net          | Width |
|-------------------|-------|--------------|-------|
| +1.8VO_EN         | 10mil | +1.8VO_BOOT  | 25mil |
| +1.8VO            | Shape | +1.8VO_COMP  | 10mil |
| +0.9VO_EN         | 10mil | +1.8VO_HG_R  | 25mil |
| +0.9VO            | Shape | +1.8VO_LG_R  | 25mil |
| +0.9VO_FB         | 10mil | +1.8VO_HG    | 25mil |
| +1.8VO --> DDQREF | 10mil | +1.8VO_LG    | 25mil |
| VTTREF            | 15mil | +1.8VO_PHASE | Shape |
| FPWM#             | 10mil | +1.8VO_SUR   | Shape |
| VCCA              | 10mil | +1.8VO_FB    | 10mil |
| DDR_PWRGD         | 10mil | +1.8VO_SS    | 15mil |
| OC_VDDQ           | 15mil | AC_BAT_SYS   | Shape |

0407\_1445

|                              |              |                                        |          |
|------------------------------|--------------|----------------------------------------|----------|
|                              |              | <b>Title : POWER_I/O_DDR &amp; VTT</b> |          |
| ASUSTeK COMPUTER INC         |              | Engineer:                              |          |
| Size                         | Project Name | Rev                                    |          |
| Custom                       | <b>S96F</b>  | 2.0G                                   |          |
| Date: Friday, April 07, 2006 |              | Sheet                                  | 83 of 96 |



0407\_1445

|                              |              |                                |          |
|------------------------------|--------------|--------------------------------|----------|
| <b>ASUS</b>                  |              | Title : POWER_I/O_+3VA & +2.5V |          |
| ASUSTek COMPUTER INC         |              | Engineer:                      |          |
| Size                         | Project Name | Rev                            |          |
| Custom                       | S96F         | 2.0G                           |          |
| Date: Friday, April 07, 2006 |              | Sheet                          | 84 of 96 |

AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN > 17.44V active

### Setting the Adapter Input Current Limit

Adapter lin(max) = [0.075V/Rsense(ADin)]\*[VCLS/VREF]  
VCLS= 2.865V

**Adaptor Max. Current :**

PR5714 = 178K; Ilimit = 4.5A; 90W  
PR5714 = 47K; Ilimit = 3.5A; 65W

### Setting the Charge Voltage

$$V_{batt} = Cell * \{ V_{ref} + [(V_{CTL} - 1.8V) / 9.52] \}$$

$$V_{CTL} = 1.588V \Rightarrow V_{batt} = 4.2V$$

### Setting the Charge Current

Charge Current Ichg =  $[0.075V/R_{sense}(CHG)]*[V_{ICTL}/3.6V]$   
 $R_{sense}(CHG) = 15m\ \Omega$

**Pre-Charging Mode :**

Precharging current = 148 ~ 152mA  
V<sub>ict1</sub> = 0.107V ~ 0.109V

### Battery Cell Selection :

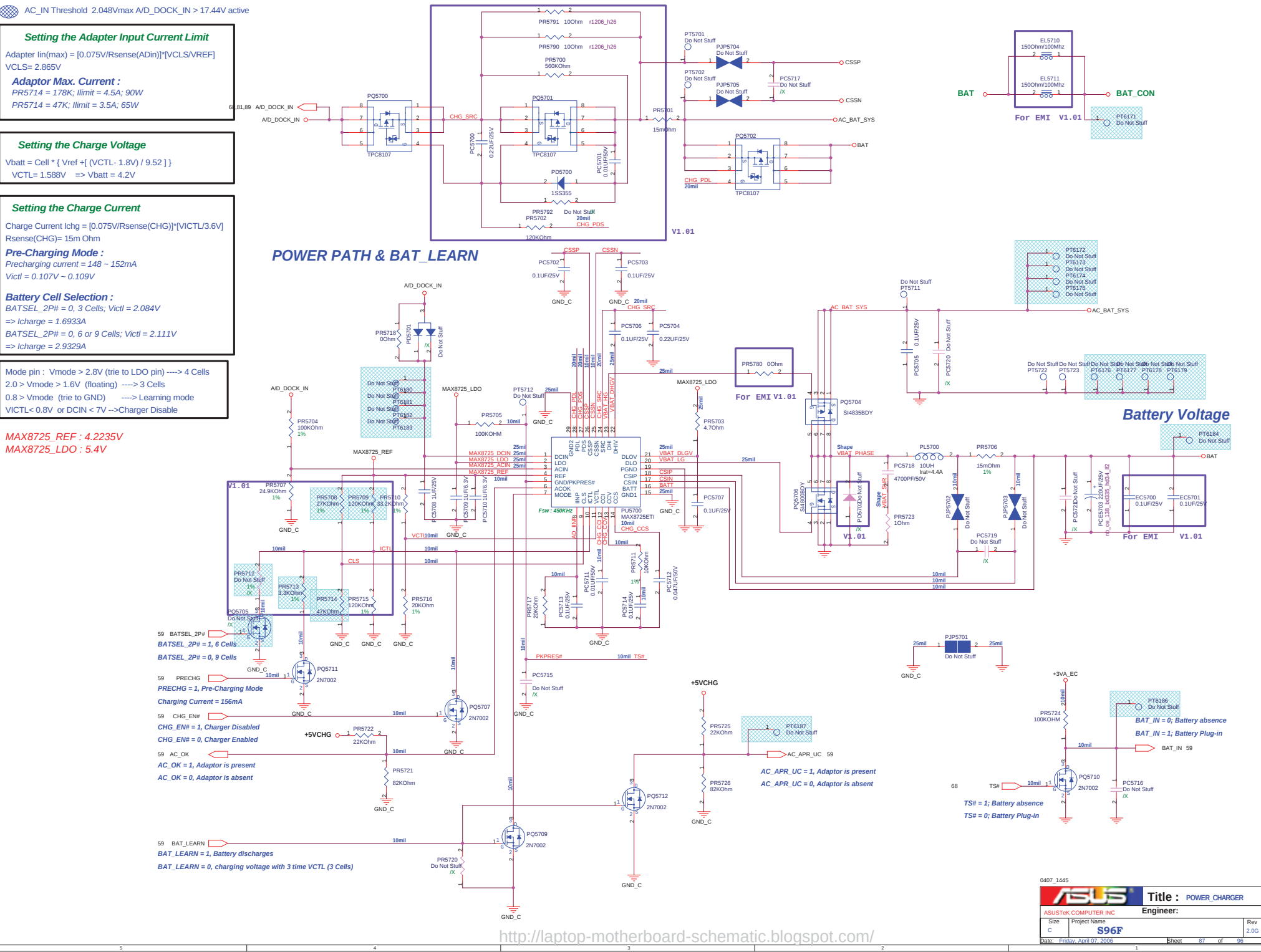
BATSEL\_2P# = 0, 3 Cells; Vct1 = 2.084V

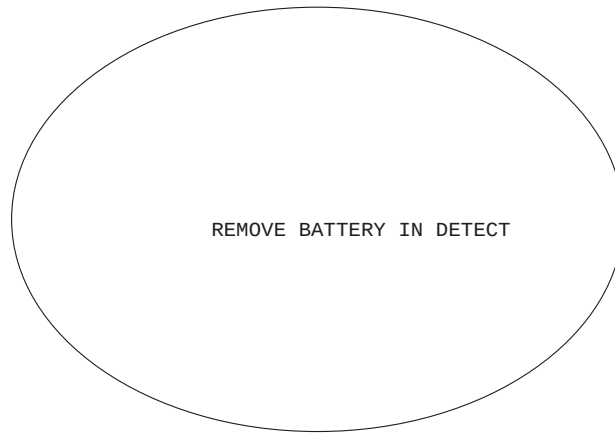
$$\Rightarrow I_{\text{charge}} = 1.6933 \text{ A}$$

BATSEL\_2P# = 0, 6 or 9 Cells; Vct1 = 2.111V  
=> Icharge = 2.9329A

Mode pin : Vmode > 2.8V (try to LDO pin) ----> 4 Cells  
2.0 > Vmode > 1.6V (floating) ----> 3 Cells  
0.8 > Vmode (try to GND) ----> Learning mode  
VICTL < 0.8V or DCIN < 7V --> Charger Disable

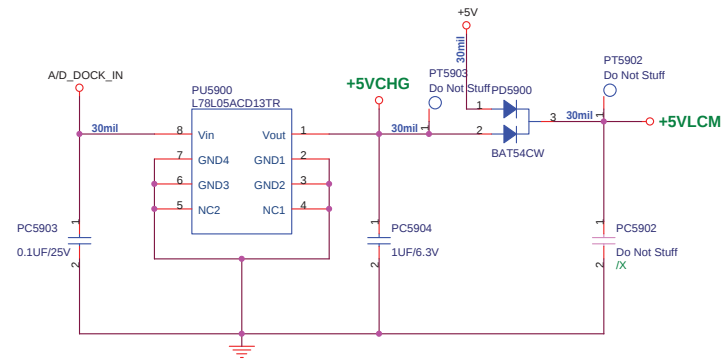
MAX8725\_REF : 4.2235V  
MAX8725\_LDO : 5.4V





REMOVE BATTERY IN DETECT

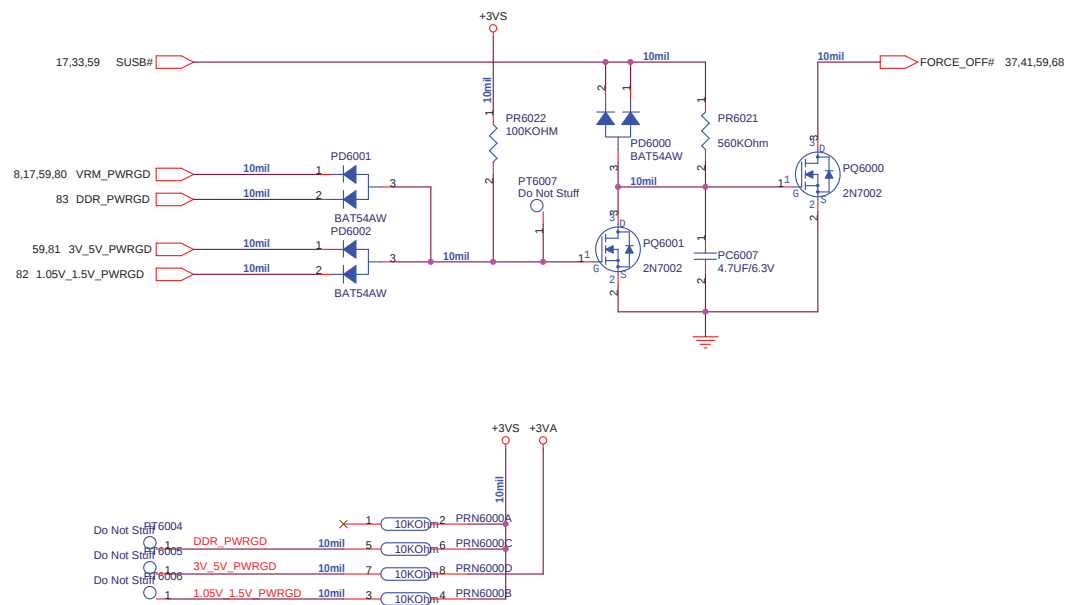
### +5VLCM / +5VCHG



0407\_1445

|                                                                                       |              |                      |       |
|---------------------------------------------------------------------------------------|--------------|----------------------|-------|
|  |              | Title : POWER_DETECT |       |
| ASUSTeK COMPUTER INC                                                                  |              | Engineer:            |       |
| Size                                                                                  | Project Name | Rev                  |       |
| Custom                                                                                | S96F         | 2.0G                 |       |
| Date: Friday, April 07, 2006                                                          | Sheet        | 89                   | of 96 |

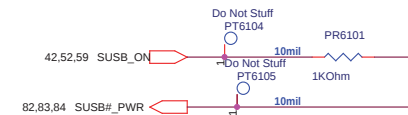
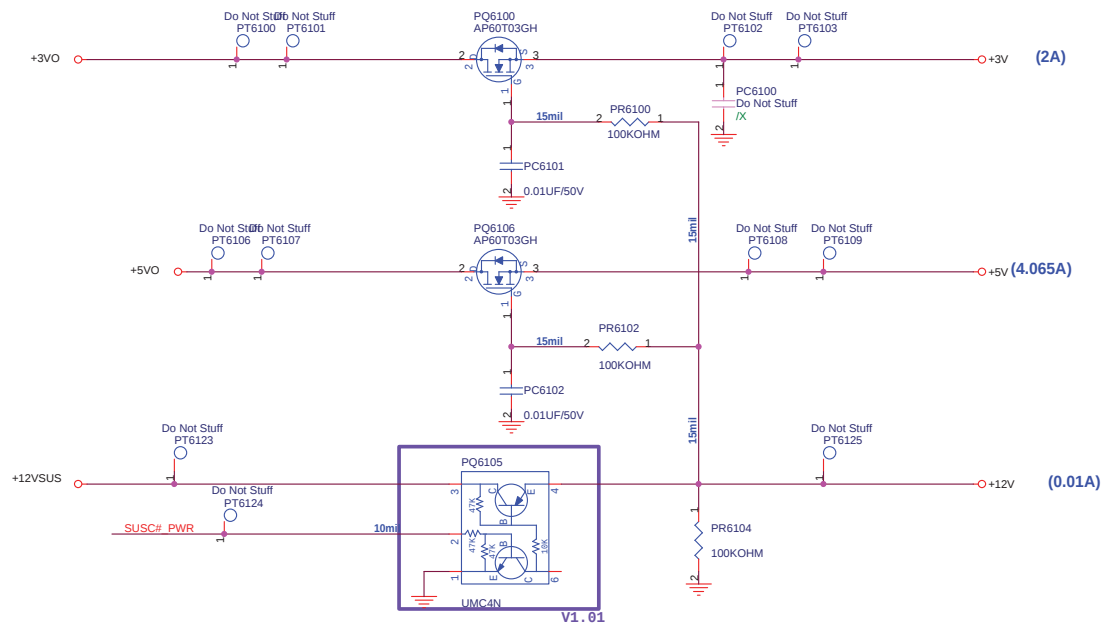
## Power Good Detector



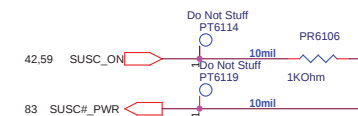
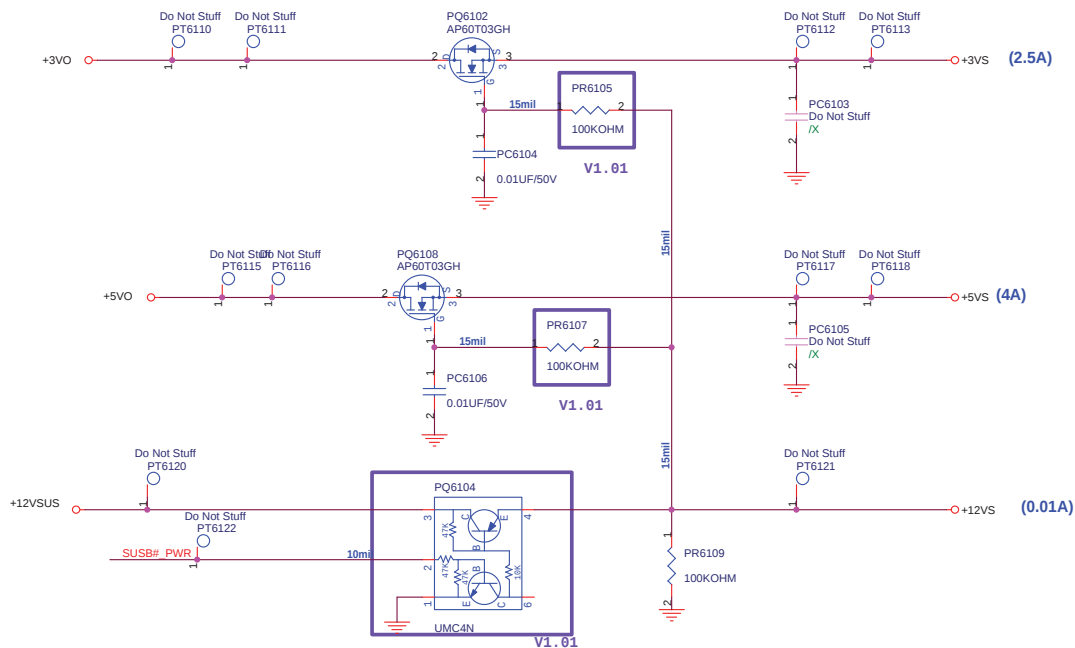
0407\_1445

|                              |              |                              |       |
|------------------------------|--------------|------------------------------|-------|
| <b>ASUS</b>                  |              | <b>Title : POWER_PROTECT</b> |       |
| ASUSTeK COMPUTER INC         |              | <b>Engineer:</b>             |       |
| Size                         | Project Name | Rev                          |       |
| Custom                       | <b>S96F</b>  | 2.0G                         |       |
| Date: Friday, April 07, 2006 | Sheet        | 90                           | of 96 |

## SUSC#\_PWR POWER

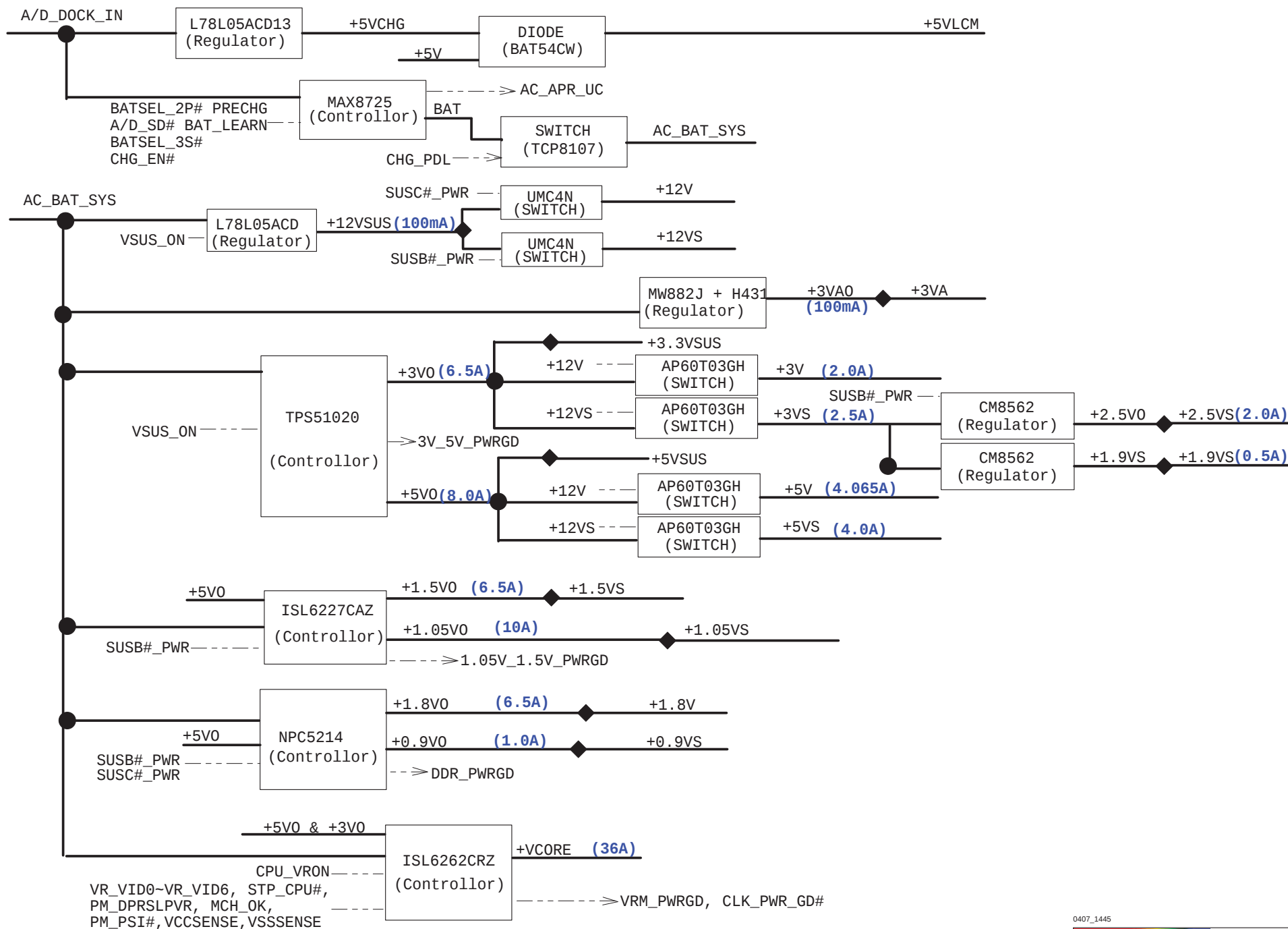


## SUSB#\_PWR POWER



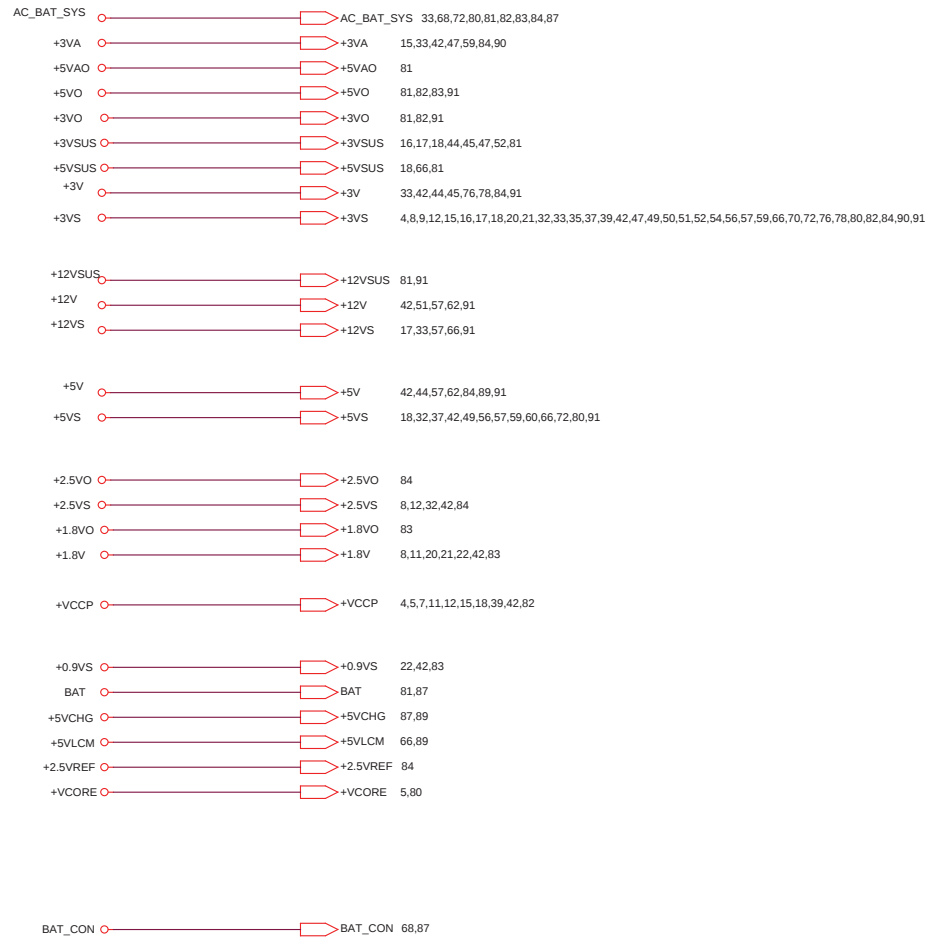
0407\_1445

|                              |              |                                  |       |
|------------------------------|--------------|----------------------------------|-------|
| <b>ASUS</b>                  |              | <b>Title : POWER_LOAD SWITCH</b> |       |
| ASUSTek COMPUTER INC         |              | Engineer:                        |       |
| Size                         | Project Name | Rev                              |       |
| Custom                       | S96F         | 2.0G                             |       |
| Date: Friday, April 07, 2006 | Sheet        | 91                               | of 96 |



0407\_1445

|                              |              |                                |       |
|------------------------------|--------------|--------------------------------|-------|
| <b>ASUS</b>                  |              | <b>Title : POWER_FLOWCHART</b> |       |
| ASUSTek COMPUTER INC         |              | Engineer:                      |       |
| Size                         | Project Name | Rev                            |       |
| Custom                       | S96F         | 2.0G                           |       |
| Date: Friday, April 07, 2006 | Sheet        | 92                             | of 96 |



0106

0407\_1445

|                                                                                       |              |                      |       |
|---------------------------------------------------------------------------------------|--------------|----------------------|-------|
|  |              | Title : POWER_SIGNAL |       |
| ASUSTek COMPUTER INC                                                                  |              | Engineer:            |       |
| Size                                                                                  | Project Name | Rev                  |       |
| Custom                                                                                | S96F         | 2.0G                 |       |
| Date: Friday, April 07, 2006                                                          | Sheet        | 93                   | of 96 |

## CIRCUIT UPDATED HISTORY

| Rev   | Date               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.00G | 2006/01/10<br>1430 | Initial release, revision 0.1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|       | 2006/01/11<br>2100 | 1. Change NB(U2) part number from 02G010009100 to 02G10009205<br>2. Change SB(U3) part number from 02G010008800 to 02G10007741<br>3. Change RN77, RN78 signals.<br>4. Swap EC(U35) pin33/36/37 signals from CLK_PWRSERVE# / T85 / FAN_PWM to FAN_PWM / CLK_PWRSERVE# / T85.<br>5. Change power circuit page 81, 82, 83, 87 (refer Z96F_R01_0111_P.DSN)<br>6. Delete T139-T141, T143-T146<br>7. Swap Network resistor signals for layout routing.                                                                                                                                                                                                                                                                                                                                 |
|       | 2006/01/12<br>0922 | 1. Swap L84, L108, L115 signals for layout routing.<br>2. Change power circuit page 84 (refer Z96F_R01_0111_P1.DSN)<br>3. Delete T142.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|       | 2006/01/13<br>1509 | 1. Add C757 for EMI request.<br>2. Modify page2 EC GPIO setting notice table.<br>3. Swap Network resistor signals for layout routing.<br>4. Change PR4724 PU from MAX8725_LDO to +3VA_EC.<br>5. Remove AC_APR_UC# from U35.28 to U35.172<br>6. Delete H41-46                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|       | 2006/01/14<br>1301 | 1. Delete: R413-R415, R417, F3, C508, R534, R303, R305, RN73-RN76, R5732-R5736.<br>2. NU(not use): C755, R5765, R5766, R5764, R5768, C71, R47, C513, C514, C707,C708, C517, C524, C526, C568, C642, C741, C744, C745, C726, C706, C404.<br>3. page32, change RGB far end terminator from Resistor(R5759/R5761/R5763) to Network Resistor(RN79).<br>4. page35, change TV_OUT signal far end terminator from Resistor(R5755-R5757) to Network Resistor(RN80).<br>5. page42, change discharge resistor from Resistor(R5774-R5783) to Network Resistor(RN81-RN83).<br>6. Change RN77 signal.<br>7. Change 25MHz X'tal (X7) to 07G010Q12500.<br>8. Change Thermal IC U16 to SOP (06G023026011)<br>9. Change 0.1UF/25V cap from X7R +/-10% to Y5V+80-20%: C757, C643, C646, C649, C652 |
|       | 2006/01/16<br>1530 | 1. Change power circuit page 80, 81, 82, 83 (refer Z96F_R00_0116_P.DSN)<br>2. Change X1, X6 package to same as Z84F.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|       | 2006/01/17<br>1046 | 1. Swap Network resistor signals for layout routing.<br>2. Change Codec ALC882(U30) part number from 02G611001300 to 02G611001310.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|       | 2006/01/17<br>2038 | 1. Change power circuit page 80, 83 (refer Z96F_R01_0117_P.DSN)<br>2. Add Network Resistor RN84, RN85(NU, reserved) to block VGA signal between CRT and PortBar connector( EMI request) .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|       | 2006/01/18<br>1103 | 1. Swap Network resistor RN81, RN83 signals for layout routing.<br>2. Stuff C755.<br>3. NU: C115, C116, R304, R306, R282, R284, R5796, CN10, C655, C656.<br>4. Add 3 0ohm resistor R5805(NU), R5806, R5807 for SATA function disable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| Rev | Date               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     | 2006/01/18<br>1645 | 1. Change power circuit page 81, 82, 83, 84, 87 (refer Z96F_R01_0118_P.DSN)<br>2. Swap PCIE clock (NEWCARD & MCH_3GPLL) for layout routing.<br>3. Swap Network resistor RN58, RN77, RN78, RN84, RN85 signals for layout routing.                                                                                                                                                                                                                    |
|     | 2006/01/19<br>1145 | 1. Swap Network resistor RN18, RN82, RN85 signals for layout routing.<br>2. Change U1 (CPU) ,U2 (North Bridge) ,U3 (South Bridge) to Note Book parts.                                                                                                                                                                                                                                                                                               |
|     | 2006/01/19<br>2127 | 1. Change power circuit page 81 (refer Z96F_R01_0119_P.DSN)                                                                                                                                                                                                                                                                                                                                                                                         |
|     | 2006/01/20<br>1735 | 1. DEL PORT_BAR.<br>2. Add an ESATA (page54) and an USB port.<br>3. Change CON27.47, CON27.48 / CON26.25, CON26.26 / CON28.54, CON28.53 to NC<br>4. Connect H35-H40, H62, H63 to GND                                                                                                                                                                                                                                                                |
|     | 2006/01/23<br>1005 | 1. Change power circuit page 80- 84, 87, 91 (refer Z96F_R01_0120_P.DSN)<br>2. DEL RN84, RN85, R5719-R5726.                                                                                                                                                                                                                                                                                                                                          |
|     | 2006/01/23<br>1714 | 1. Change power circuit page 84, 87, 91 (refer Z96F_R01_0120_P1.DSN)<br>2. Change ESATA1/ CON42 connector to NB part.<br>3. Change EC(U35) pin 28 from T174 to AC_APR_UC# signal.<br>4. Change EC(U35) pin 174 signal from AC_APR_UC# to AC_OK# signal.<br>5. Add a N-MOS(Q6118) to invert AC_OK signal.                                                                                                                                            |
|     | 2006/01/24<br>1030 | 1. Change RN53, RN54, RN81-RN83 from 0402 to 0603.<br>2. Add C764-765, R5812-5815 for ESATA.<br>3. Add D59, Q6119 to switching XD card power.<br>4. Change CON21 signal.<br>5. Change U35.89/RN41.1/SW3.1/SW3.2 signal from EXPLORE_SW# to PWR4GEAR#.<br>6. Change power circuit page 81 (refer Z96F_R01_0124_P.DSN)<br>7. Swap Network resistor RN18, RN79, RN78, L115 signals for layout routing.<br>8. Change page 93 +5VA signal name to +5VAO. |
|     | 2006/01/25<br>1425 | 1. Change RN70, RN71, RN79, RN80 to LF parts.<br>2. Change PU5700.6 signal name to AC_OK.                                                                                                                                                                                                                                                                                                                                                           |
|     | 2006/01/25<br>2110 | 1. Swap Network resistor RN33, RN53, RN70, RN79, RN80 signals for layout routing.<br>2. Change T2R2 to 10M ohms.                                                                                                                                                                                                                                                                                                                                    |
|     | 2006/01/26<br>1822 | Change Revision to 1.00G                                                                                                                                                                                                                                                                                                                                                                                                                            |
|     | 2006/02/13<br>1536 | Change C764, C765, C118-C121 from Y5V to X7R<br>Change T2C25, T2C26 from Y5V to X7R                                                                                                                                                                                                                                                                                                                                                                 |
|     | 2006/02/17<br>1639 | Modify Block Diagram                                                                                                                                                                                                                                                                                                                                                                                                                                |

0407\_1445

|                                                                                       |              |                    |          |
|---------------------------------------------------------------------------------------|--------------|--------------------|----------|
|  |              | Title : History(1) |          |
| ASUSTek COMPUTER INC                                                                  |              | Engineer: Mike Lee |          |
| Size                                                                                  | Project Name | Rev                |          |
| Custom                                                                                | S96F         | 2.0G               |          |
| Date: Friday, April 07, 2006                                                          |              | Sheet              | 94 of 96 |

## CIRCUIT UPDATED HISTORY(2)

| Rev          | Date               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1.01G</b> | 2006/02/27<br>1100 | 1. Change R5710 to NU<br>2. Add R5816(NU)<br>3. Change page54 ESATA power from +VRAM to +1.8V<br>4. Change C717, C718 connection.<br>5. Swap INTERNAL MIC R/L.<br>6. Stuff R47 (10M ohms).<br>7. Change Rev to 1.01G                                                                                                                                                                                                                                 |
|              | 2006/03/01<br>1120 | 1. Add R5828-5831, C788.<br>2. Swap LTPB0-/+ common choke (L112) for routing.<br>3. Swap LTPA0-/+ common choke (L113) for routing.<br>4. Swap USB_PN5/_PP5 common choke (L115) for layout routing.<br>5. Swap RN34 signals for layout routing.<br>6. Change page54 ESATA from SI13132 to JMB360.<br>7. Change page74 scrow hole type.                                                                                                                |
|              | 2006/03/02<br>1819 | 1. Updated power page80-84, 87, 91<br>2. Del page55 circuit.                                                                                                                                                                                                                                                                                                                                                                                         |
|              | 2006/03/03<br>1450 | 1. Add screw hole H63<br>2. Change ESATA SMBus PU 4.7K to 3V<br>3. Change ESATA +1.8V to +1.9V<br>4. Modify page54 ESATA power rail.<br>5. Updated power circuit page80-82, 84, 87.<br>6. Change HSYNC/VSYN level shifter (U44, U45) power rail from 5V to 3.3V.                                                                                                                                                                                     |
|              | 2006/03/03<br>1740 | 1. Updated power circuit page80-82, 84, 87 (refer Z96F_R101G_0303_P2.DSN).<br>2. Add PWRSW# mask circuit (page41).<br>3. Change HSYNC/VSYN ESD power rail from 5V to 3.3V.                                                                                                                                                                                                                                                                           |
| <b>1.1G</b>  | 2006/03/06<br>1950 | 1. Change H54, H56 / H29, H31 / H3 / H33 from screw hole to NUTs.<br>2. Change X1 / X6 from DIP type to SMD type.<br>3. Change C112, C113 / C632, C633 value from 20pF to 12pF.<br>4. For EMI:<br>1) Add L124.<br>2) Change R536, R537 from 0R to Bead(1K ohm/100MHz).<br>3) Stuff R418, R431 with 0R.<br>4) Change L52 from 80 ohm/100MHz to 150ohm/100MHz).<br>5) Stuff C411, C412, C413, C414.<br>5. Change Rev to 1.1G (to meet NB team PN rule) |
|              | 2006/03/08<br>1100 | 1. Del H23<br>2. Del C698, C699<br>3. Add RN73-76, C793-799 (NU, for EMI).<br>4. NU R359                                                                                                                                                                                                                                                                                                                                                             |
|              | 2006/03/09<br>2121 | 1. Swap RN44, RN54 signals for routing.<br>2. Stuff R5794, RTC BATT, R68, R69, C517, C524, C526, R550<br>3. NU R71, R72, R307<br>4. Change D58 from SS0540 to 1N4148<br>5. Change CON5 (LVDS CONN) to 12G09103004P<br>6. Change U16 to ADT7461ARMZ<br>7. Change SW1-4, SW6-7 to 12G09103004P                                                                                                                                                         |

| Rev | Date               | Description                                                                                                                                                                                                                                                                                                     |
|-----|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                    | 8. Change X7 part.<br>9. Change C727-728 from 24p to 18p<br>10. NU R5770, R5769, Q6116, SW11, R5717, R5718<br>11. Add C500 for U23<br>12. Del XD function: Del D59, Q6119, C709.                                                                                                                                |
|     | 2006/03/10<br>1212 | 1. Change power circuit page 81-84, 87 (refer Z96F_R11_0310_P.DSN)                                                                                                                                                                                                                                              |
|     | 2006/03/10<br>1538 | 1. NC CON36.16                                                                                                                                                                                                                                                                                                  |
|     | 2006/03/13<br>2013 | 1. Change R48 from 22K to 100K<br>2. Del R307.<br>3. NU R5795, Q6117, R550.<br>4. Stuff R5797=0R, SW7.                                                                                                                                                                                                          |
|     | 2006/03/14<br>1430 | 1. Change U1 to 12G04600479A<br>2. Change CON2 to 12G025332003<br>3. Change CON3 to 12G025122000<br>4. Change CON36 to 12G142101100<br>5. Change CON27 to 12G161530444<br>6. Change CON13 to 12G030100522<br>7. Change J1, J2 to 12G140031067<br>8. Change power circuit page 81, 82(refer Z96F_R11_0314_P.DSN) |
|     | 2006/03/16<br>2016 | 1. Stuff CE2 100UF/2.5V_7343<br>2. Stuff R307 10K ohm_0402<br>3. Stuff C627, C741 10UF/10V_0805<br>4. Stuff C742, C743, C744, C748 0.1UF/16V_0402                                                                                                                                                               |
|     | 2006/04/03<br>0809 | 1. Change to Rev 2.0<br>2. Add a MOSFET Q6121 to block USB power<br>3. Add R5838, C800-C805, D61<br>4. Change NUT H56, H54 to 4.2mm<br>5. Change PR5709 P/N<br>6. Change JRST1 footprint to R0402                                                                                                               |
|     | 2006/04/03<br>1527 | 1. Change JRST1<br>2. Change power circuit page 80-84, 87, 89-92(refer Z96F_R20_0403_P.DSN)                                                                                                                                                                                                                     |
|     | 2006/04/04<br>0756 | 1. Change NEWCARD_CLK from U18.24-25 to U18.19-20<br>2. Add R5839, R5840, R5841<br>3. Add R5842, R5843, R5844<br>4. Stuff R5833<br>5. NU Q6120, R5832, R5834, R5834, D60                                                                                                                                        |
|     | 2006/04/04<br>0756 | 1. Add Stitch cap C806-C810<br>2. Add C811-C814<br>3. NU R352, Stuff R353<br>4. Change CON7.6 to GND<br>5. BIOS1 to SMD and NU U38 (BIOS Socket).                                                                                                                                                               |
|     | 2006/04/07<br>1445 | 1. Change power circuit page 84(refer Z96F_R20_0407_P.DSN)                                                                                                                                                                                                                                                      |

0467\_1445

|                                                                                       |              |                      |       |
|---------------------------------------------------------------------------------------|--------------|----------------------|-------|
|  |              | Title : History(2)   |       |
| ASUSTek COMPUTER INC                                                                  |              | Engineer: <OrgAddr1> |       |
| Size                                                                                  | Project Name | Rev                  |       |
| Custom                                                                                | S96F         | 2.0G                 |       |
| Date: Friday, April 07, 2006                                                          | Sheet        | 95                   | of 96 |